



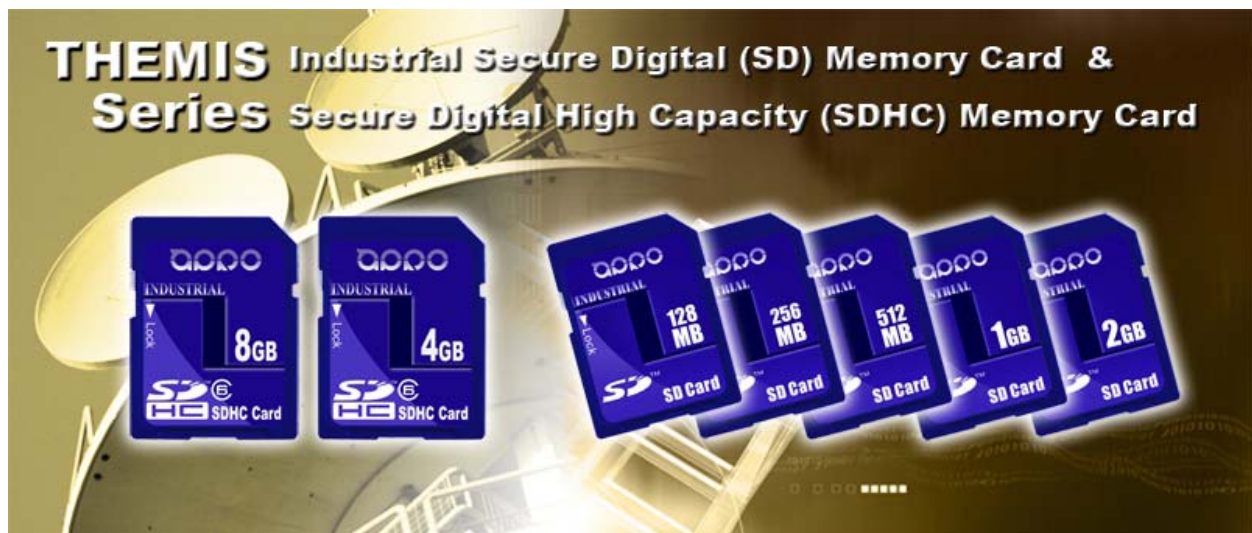
April 2012

Product Specification

Industrial SD & SDHC Memory Cards

– THEMIS Series –

Doc-No: 100-WPSDx-EASL-1V4



This document is for information use only and is subject to change without prior notice. APRO Co., Ltd. Assumes no responsibility for any errors that may appear in this document, nor for incidental or consequential damages resulting from the furnishing, performance or use of this material. No part of this document may be reproduced, transmitted, transcribed, stored in a retrievable manner or translated into any language or computer language, in any form or by any means, electronic, mechanical, magnetic, optical, chemical, manual or otherwise, without the prior written consent of an officer of APRO Co., Ltd..

All parts of the APRO documentation are protected by copyright law and all rights are reserved.

APRO and the APRO logo are registered trademarks of APRO Co., Ltd.

Product names mentioned herein are for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

© 2012 APRO Corporation. All rights reserved.

Revision History

| Rev. | Description | Update |
|-------------|-------------------------------|---------------|
| 1.0 | Initial release | 2010/12/22 |
| 1.1 | Typo correction | 2010/12/23 |
| 1.2 | File allocation table updated | 2011/05/25 |
| 1.3 | General revise | 2011/11/28 |
| 1.4 | General revise | 2012/4/25 |

CONTENTS

| | |
|---|---------------|
| 1. INTRODUCTION..... | - 1 - |
| 1.1. SCOPE..... | - 2 - |
| 1.2. SYSTEM FEATURES..... | - 2 - |
| 1.3. SD CARD STANDARD..... | - 2 - |
| 1.4. FUNCTIONAL DESCRIPTION | - 3 - |
| 1.4.1. Technology Independence..... | - 3 - |
| 1.4.2. Wear Leveling..... | - 3 - |
| 1.4.3. Flash Memory Access | - 3 - |
| 1.4.4. Management of Flash Memory Defects | - 3 - |
| 1.4.5. Error Recovery..... | - 4 - |
| 2. PRODUCT SPECIFICATIONS | - 5 - |
| 2.1. SD CARD SPECIFICATIONS | - 5 - |
| 2.2. SYSTEM ENVIRONMENTAL SPECIFICATIONS | - 5 - |
| 2.3. SYSTEM POWER REQUIREMENTS | - 5 - |
| 2.4. SYSTEM PERFORMANCE | - 6 - |
| 2.5. SYSTEM RELIABILITY | - 6 - |
| 2.6. PHYSICAL SPECIFICATIONS | - 6 - |
| 2.7. CAPACITY SPECIFICATIONS | - 8 - |
| 3. SD & SDHC MEMORY CARD INTERFACE DESCRIPTION | - 8 - |
| 3.1. PHYSICAL DESCRIPTION | - 8 - |
| 3.1.1. Pin Assignments in Industrial Grade SD Memory Card and SDHC Memory Card Mode | - 8 - |
| 3.1.2. Pin Assignments in SPI Mode | - 9 - |
| 3.2. SD BUS TOPOLOGY | - 11 - |
| 3.3. SPI BUS TOPOLOGY..... | - 12 - |
| 4. ELECTRICAL SPECIFICATIONS | - 14 - |
| 4.1. DC CHARACTER..... | - 14 - |
| 4.2. BUS SIGNAL LINE LOADING | - 14 - |
| 4.3. AC CHARACTERISTICS | - 14 - |
| 4.3.1. Bus Signal Levels | - 14 - |
| 4.3.2. Bus Timing (SD Default Mode) | - 16 - |
| 4.3.3. But Timing (Default) – Low speed mode timing | - 17 - |
| 5. REGISTER TABLE..... | - 18 - |
| 5.1. OPERATION CONDITION REGISTER (OCR)..... | - 18 - |

5.2. **CARD IDENTIFICATION REGISTER (CID)**..... - 19 -

5.3. **DRIVER STAGE REGISTER (DSR)**..... - 19 -

5.4. **RELATIVE CARD ADDRESS REGISTER (RCA)**..... - 19 -

5.5. **CARD SPECIFIC DATA REGISTER (CSD)**..... - 19 -

5.6. **SD 2.0 CSD FOR HIGH CAPACITY CARD TABLE (4GB AND 8GB)**..... - 20 -

5.7. **SD 2.0 CSD FOR STANDARD CAPACITY CARD TABLE (128MB TO 2GB)**..... - 21 -

5.8. **SD 1.1 CSD TABLE**..... - 22 -

5.9. **SD 1.01 CSD TABLE**..... - 23 -

5.10. **SD CARD CONFIGURATION REGISTER (SCR)**..... - 24 -

6. **SD & SDHC MEMORY CARD PROTOCOL DESCRIPTION**..... - 25 -

6.1. **SD BUS PROTOCOL** - 25 -

7. **SPI PROTOCOL DEFINITION** - 29 -

7.1. **SPI BUS PROTOCOL**..... - 29 -

7.1.1. **Data Read**..... - 29 -

7.1.2. **Data Write** - 30 -

APPENDIX A. ORDERING INFORMATION..... - 32 -

APPENDIX B. LIMITED WARRANTY - 33 -

List of Tables

| | |
|---|--------|
| TABLE 1: SDA SPECIFICATION..... | - 5 - |
| TABLE 2: ENVIRONMENTAL SPECIFICATION | - 5 - |
| TABLE 3: SYSTEM POWER REQUIREMENT | - 5 - |
| TABLE 4: SYSTEM PERFORMANCES | - 6 - |
| TABLE 5: SYSTEM RELIABILITY..... | - 6 - |
| TABLE 6: PHYSICAL SPECIFICATIONS..... | - 6 - |
| TABLE 7: MODEL CAPACITY | - 8 - |
| TABLE 8: SD BUS MODE PIN DEFINITION..... | - 9 - |
| TABLE 9: SPI BUS MODE PIN DEFINITION | - 9 - |
| TABLE 10: SD CARD REGISTERS | - 10 - |
| TABLE 11: GENERAL DC CHARACTER | - 14 - |
| TABLE 12: BUS SIGNAL LINE LOADING | - 14 - |
| TABLE 13: BUS SIGNAL LEVEL..... | - 15 - |
| TABLE 14: INPUT AND OUTPUT VOLTAGES | - 15 - |
| TABLE 15: HIGH-SPEED MODE TIMING | - 16 - |
| TABLE 16: BUS TIMING-PARAMETERS VALUES (DEFAULT)..... | - 17 - |
| TABLE 17: REGISTER NAME V.S. SD SPECIFICATION..... | - 18 - |
| TABLE 18: OCR TABLE..... | - 18 - |
| TABLE 19: CID TABLE | - 19 - |
| TABLE 20: SD 2.0 CSD FOR HIGH CAPACITY CARD TABLE (4GB AND 8GB) | - 20 - |
| TABLE 21: SD 2.0 CSD FOR HIGH CAPACITY CARD TABLE (128MB AND 2GB) | - 21 - |
| TABLE 22: SD 1.1 CSD TABLE | - 22 - |
| TABLE 23: SD 1.01 CSD TABLE | - 23 - |
| TABLE 24: SCR TABLE..... | - 24 - |

List of Figures

| | |
|--|--------|
| FIGURE 1: INDUSTRIAL GRADE SD & SDHC MEMORY CARD BLOCK DIAGRAM | - 1 - |
| FIGURE 2: SD & SDHC MEMORY CARD DIMENSIONS (1 OUT OF 3)..... | - 7 - |
| FIGURE 3: SD & SDHC MEMORY CARD DIMENSIONS (2 OUT OF 3)..... | - 7 - |
| FIGURE 4: SD & SDHC MEMORY CARD DIMENSIONS (3OUT OF 3)..... | - 8 - |
| FIGURE 5: INDUSTRIAL GRADE SD CARD ARCHITECTURE..... | - 10 - |
| FIGURE 6: INDUSTRIAL GRADE SD CARD SYSTEM BUS TOPOLOGY | - 11 - |
| FIGURE 7: BUS CIRCUITRY DIAGRAM | - 12 - |
| FIGURE 8: INDUSTRIAL GRADE SD CARD BUS SYSTEM | - 13 - |
| FIGURE 9: BUS SIGNAL LEVELS | - 14 - |
| FIGURE 10: TIMING DIAGRAM DATA INPUT/OUTPUT REFERENCED TO CLOCK (HIGH-SPEED) | - 16 - |
| FIGURE 11: TIMING DIAGRAM DATA INPUT/OUTPUT REFERENCED TO CLOCK (DEFAULT) | - 17 - |
| FIGURE 12: “NO RESPONSE” AND “NO DATA” OPERATIONS | - 25 - |
| FIGURE 13: MULTIPLE BLOCK READ OPERATION | - 26 - |
| FIGURE 14: MULTIPLE BLOCK WRITE OPERATION | - 26 - |
| FIGURE 15: COMMAND TOKEN FORMAT | - 26 - |
| FIGURE 16: RESPONSE TOKEN FORMAT | - 27 - |
| FIGURE 17: DATA PACKET FORMAT | - 28 - |
| FIGURE 18: SINGLE BLOCK READ OPERATION | - 29 - |
| FIGURE 19: READ OPERATION—DATA ERROR | - 30 - |
| FIGURE 20: MULTIPLE BLOCK READ OPERATION | - 30 - |
| FIGURE 21: SINGLE BLOCK WRITE OPERATION..... | - 31 - |
| FIGURE 22: MULTIPLE BLOCK WRITE OPERATION | - 31 - |

1. Introduction

The APRO Industrial Grade SD & SDHC Memory Card in THEMIS Series is NAND-SLC Flash based memory card that is specifically designed to meet the security, performance and environmental requirements of some significant applications such like networking, telecommunications and data-communications, mobile & embedded computing, medical instruments and industrial computing applications. The APRO Industrial Grade SD & SDHC Memory Cards include a copyright protection that complies with the security of the SDMI standard, and the physical form-factor, pin assignment and data transfer protocol are forward compatible with SD & SDHC Memory Card, with some additions.

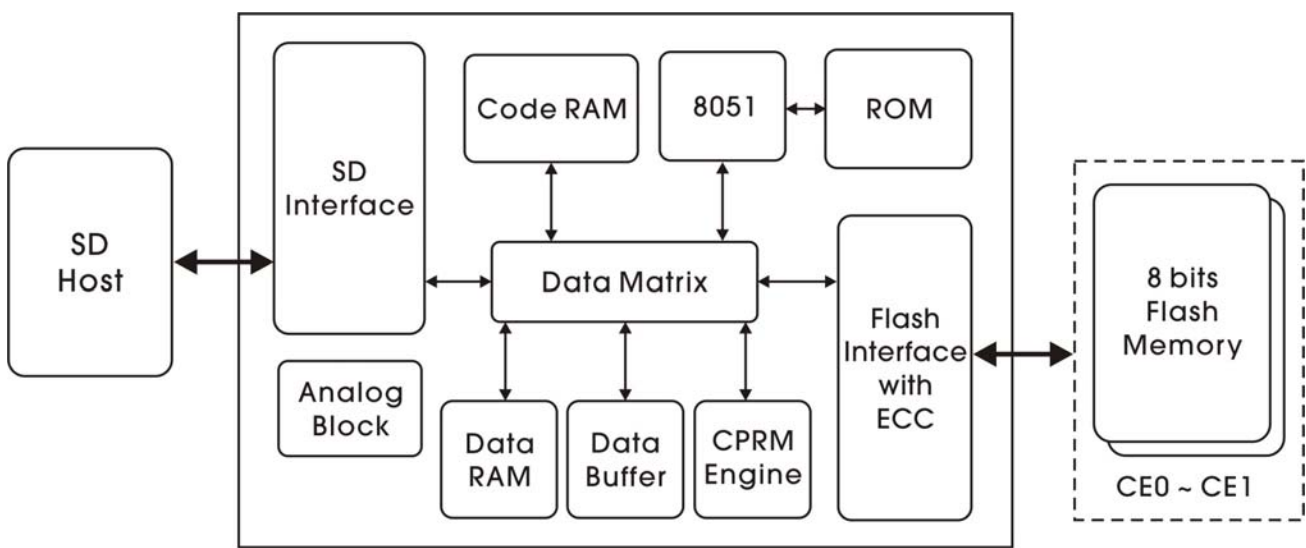


Figure 1: Industrial Grade SD & SDHC Memory Card Block Diagram

1.1. **Scope**

This document describes the key features and specifications of APRO Industrial Grade SD & SDHC Memory Cards in THEMIS Series, as well as the information required to interface this product to a host system.

1.2. **System Features**

- NAND type SLC Flash technology
- Capacities from 128MB~2GB are compliant with SD v1.01 / v1.1 / v2.0 specifications
- Capacities of 4GB & 8GB are compliant with SD v1.01 / v1.1 / v2.0 / v3.0 specifications
- 9 exposed contacts on one side
- Supports industrial grade operating temperature -40°C to +85°C
- SD Memory Card capacity from 128MB to 2GB and SDHC Memory Card from 4GB to 8GB
- SD Card protocol compatible
- Supports SD mode and SPI mode
- Supports CPRM
- Copyright Protection Mechanism-Complies with highest security of SDMI standard
- Write protect feature using mechanical switch
- SD performance up to 19.98 MB/sec; SDHC performance up to 20.09 MB/sec
- RoHS & REACH compliant

1.3. **SD Card Standard**

APRO Industrial Grade SD & SDHC Memory Cards are fully compatible with the following SD physical Layer Specification standard:

SD & SDHC Memory Card Specifications, Part 1, Physical Layer Specification, Version 2.00

This specification may be obtained from:

SD Card Association
53 Muckelemi St.
P.O. Box 189
San Juan Bautista, CA 95045-0189
USA
Phone : 831-623-2107
Fax : 831-623-2248
<http://www.sdcard.org>

1.4. Functional Description

APRO's THEMIS Series Industrial Grade SD and SDHC memory cards contain a high level and intelligent subsystem as shown in Figure 1. This intelligent SD & SDHC Memory Card controller manages interfaced protocols and data storage and retrieval as well as Error Correction Code (ECC) algorithms, defect handling and diagnostics, power management related functions. For SD and SDHC memory cards, Content Protection for Recordable Media (CPRM) related function is also included.

1.4.1. Technology Independence

The 512-byte sector size of the SD & SDHC Memory Card is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues a Read or Write command to the SD & SDHC Memory Card. This command contains the address and the number of sectors to write/read. The host software then waits for the command to complete. The host software does not get involved in the details of how the flash memory is erased, programmed or read. This is extremely important as flash devices are expected to get more and more complex in the future. Since the SD & SDHC Memory Card Titans Series uses an intelligent on-board controller, the host system software will not require changing as new flash memory evolves. In other words, systems that support the SD & SDHC Memory Card today will be able to access future APRO cards built with new flash technology without having to update or change host software.

1.4.2. Wear Leveling

Wear Leveling is an intrinsic part of the Erase Pooling functionality of APRO industrial SD & SDHC Memory Cards using NAND type SLC flash memory. The WEAR LEVELING command is supported to ensure the best of flash memory endurance capability. The THEMIS Series industrial SD & SDHC memory cards support global wear-leveling algorithms.

1.4.3. Flash Memory Access

To write or read a sector (or multiple sectors), the master (host device) simply issues a read or a write command set to the SD and SDHC Memory Card Controller. The command set contains the address and related information about the access characteristics. The master (host device) does not get involved in the details of how the flash memory is erased, programmed or read.

1.4.4. Management of Flash Memory Defects

APRO Industrial SD & SDHC Memory Cards also contain a sophisticated defect and error management system. The SD & SDHC Memory Card controller does a read after write under margin conditions to verify that the data is written correctly (except in the case of write pre-erased sectors). In case that a bit is found to be defective, the SD & SDHC Memory Card Controller replaces this bad bit with a spare bit within the sector header. If necessary, the SD & SDHC Memory Card Controller will even replace the entire sector with a spare sector. This is completely transparent to the master (host device) and does not consume any user data space.

1.4.5. Error Recovery

In the rare case a read error does occur, the SD & SDHC Memory Card Controller has an innovative algorithm to recover the data. The last line of defense is to employ a powerful ECC to correct the data. If ECC is used to recover data, defective bits are replaced with spare bits to ensure they do not cause any future problems.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. SD Card Specifications

Table 1: SDA specification

| | SD Memory Card | SDHC Memory Card |
|-----------------------|--|---|
| SD Card Specification | Capacities from 128MB~2GB are compliant with SD v1.01 / v1.1 / v2.0 specifications | Capacities of 4GB & 8GB are compliant with SD v1.01 / v1.1 / v2.0 / v3.0 specifications |
| SD Card Capacity | 128MB up to 2GB | 4GB and 8GB |
| File System | FAT | FAT32 |

2.2. System Environmental Specifications

Table 2: Environmental Specification

| | | |
|----------------|---|--|
| Temperature | Operating: Non-operating: | -40°C ~ +85°C -50°C ~ +95°C |
| Humidity | Operating & Non-operating: | 10% ~ 95% non-condensing |
| Vibration | Operating & Non-operating: | 15G compliance to MIL-STD-810F |
| Shock | Operating & Non-operating: | 1,000 G compliance to MIL-STD-810F |
| ESD Protection | Contact Pads : Non Contact Pads Area : | ±4kV, Human body model according to ANSI EOS/ESD-S5.1-1998 ±8kV (coupling plane discharge) ±15kV (air charge), Human body model per IEC61000-4-2 |
| Altitude | Operating & Non-operating: | 80,000 feet |

2.3. System Power Requirements

Table 3: System Power Requirement

| Biggest Capacity | DC Input Voltage (VCC) : 3.3V | | |
|---------------------------|-------------------------------|------------------|-------------------|
| | IDLE | Reading | Writing |
| SD Card SLC Flash – 2GB | 90uA (0.297mW) | 29.2mA (96.36mW) | 35.8mA (118.14mW) |
| SDHC Card SLC Flash – 8GB | 160uA (0.528mW) | 30.0mA (99.00mW) | 37.5mA (123.75mW) |

2.4. System Performance

Table 4: System Performances

| Card type | SD Card | | | | | SDHC Card | |
|--------------------------|---------|-------|-------|-------|-------|-----------|-------|
| | 128MB | 256MB | 512MB | 1GB | 2GB | 4GB | 8GB |
| Capacity | | | | | | | |
| Sequential Read (MB/sec) | 17.90 | 18.80 | 18.30 | 17.00 | 19.20 | 19.40 | 19.40 |
| Sequential Write(MB/sec) | 8.10 | 10.60 | 10.80 | 13.90 | 15.30 | 15.10 | 15.10 |
| The number of Flash IC | 1 | 1 | 1 | 1 | 1 | 1 | 2 |

Note:

(1) All values quoted are typically at 25°C and nominal supply voltage

(2) The Max. Performance was tested by HDBENCH MARK

(3) The performance would be different for the flash chip models and PC system's configuration

2.5. System Reliability

Table 5: System Reliability

| | |
|--------------------------|---|
| Durability | 10,000 inserting cycles |
| Bending | 10N |
| Torque | 0.15 N +/- 2.5 deg. |
| Drop Test | 1.5M free fall |
| WP Switch Cycle | 1,000 cycles @ slide force 0.4N to 5N |
| Wear-leveling Algorithms | Global wear-leveling algorithms |
| MTBF | > 3,000,000 hours |
| ECC Technology | 16 bits or 24 bits per 1Kbytes or 24 bits per 512 bytes |
| Endurance | > 2,000,000 cycles logically contributed by wear-leveling and advanced bad sector management algorithms |
| Data Retention | 10 years |

2.6. Physical Specifications

Refer to Table 6 and see Figure 2 ~ Figure 4 for SD & SDHC Memory Card physical specifications and dimensions.

Table 6: Physical Specifications

| Industrial SD & SDHC Memory Card | |
|----------------------------------|-----------------------|
| Width: | 32.00±0.10mm(1.26 in) |
| Length: | 24.00±0.10mm(0.95 in) |
| Thickness: | 2.1±0.15mm(0.08 in) |
| Weight: | 2.5g (0.09oz) Max. |

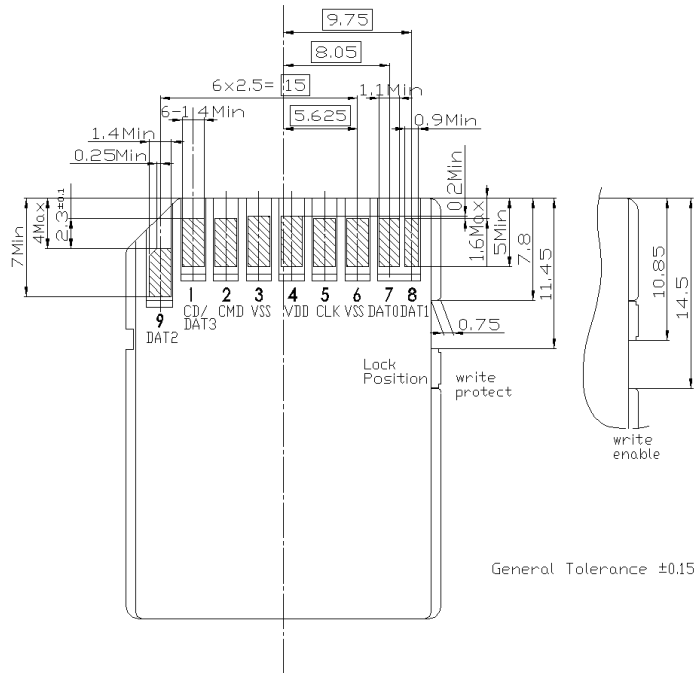


Figure 2: SD & SDHC Memory Card Dimensions (1 out of 3)

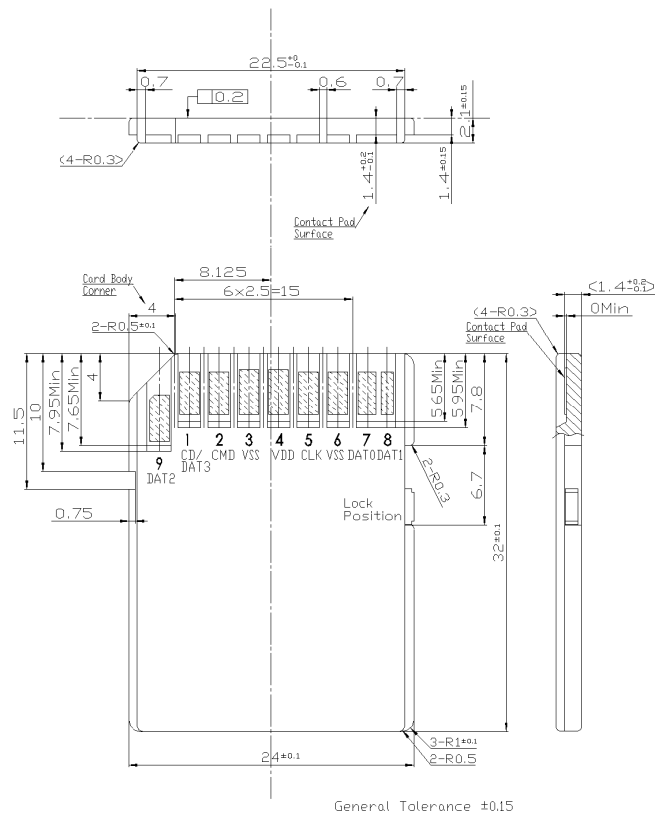


Figure 3: SD & SDHC Memory Card Dimensions (2 out of 3)

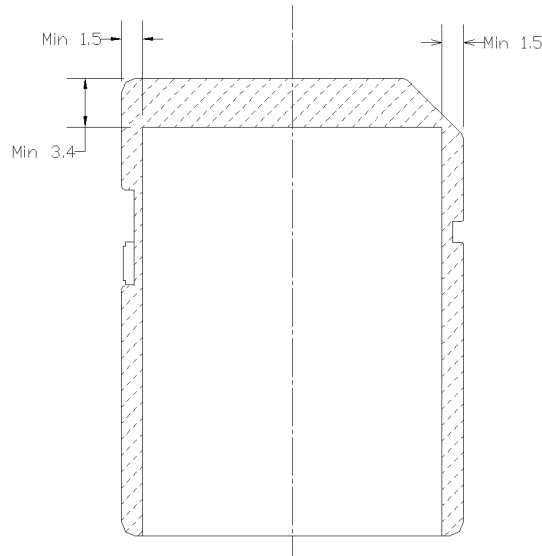


Figure 4: SD & SDHC Memory Card Dimensions (3out of 3)

2.7. Capacity Specifications

APRO Industrial SD & SDHC Memory Card is built-in mainly Samsung NAND Type SLC Flash memory chips. The table 7 shows the specific capacity for the various models and the default number of heads, sectors/track and cylinders.

Table 7: Model Capacity

| Unformatted Capacity | Cylinder | Head | Default Sector | LBA |
|----------------------|----------|------|----------------|---------------|
| 128MB | 15 | 255 | 63 | 123,379,200 |
| 256MB | 31 | 255 | 63 | 254,983,680 |
| 512MB | 62 | 255 | 63 | 509,967,360 |
| 1GB | 124 | 255 | 63 | 1,019,934,720 |
| 2GB | 250 | 255 | 63 | 2,056,320,000 |
| 4GB | 499 | 255 | 63 | 4,104,414,720 |
| 8GB | 998 | 255 | 63 | 8,208,829,440 |

3. SD & SDHC Memory Card Interface Description

3.1. Physical Description

APRO Industrial Grade SD & SDHC Memory Card has nine exposed contacts on one side (see Figure 2 and Figure 3). The host is connected to the SD Card using a dedicated 9-pin connector.

3.1.1. Pin Assignments in Industrial Grade SD Memory Card and SDHC Memory Card Mode

The signal/pin assignments and definitions in SD Card Mode are listed in below Table 8.

Table 8: SD Bus Mode Pin Definition

| Pin # | Name | Type1 | SD Description |
|-------|--------|-------|-------------------------------|
| 1 | CD/DAT | I/O3 | Card Detect/Data Line [Bit 3] |
| 2 | CMD | I/O | Command/Response |
| 3 | VSS1 | S | Supply voltage ground |
| 4 | VDD | S | Supply voltage |
| 5 | CLK | I | Clock |
| 6 | VSS2 | S | Supply voltage ground |
| 7 | DAT0 | I/O | Data Line [Bit 0] |
| 8 | DAT1 | I/O | Data Line [Bit 1] |
| 9 | DAT2 | I/O | Data Line [Bit 2] |

- Notes:
- 1) S=power supply; I=input; O=output using push-pull drivers.
 - 2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after the SET_BUS_WIDTH command. It is the responsibility of the host designer to connect external pullup resistors to all data lines even if only DAT0 is to be used. Otherwise, non-expected high current consumption may occur due to the floating inputs of DAT1 & DAT2 (in case they are not used).
 - 3) After power up, this line is input with 50Kohm(+/-20Kohm) pull-up (can be used for card detection or SPI mode selection). The pull-up may be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

3.1.2. Pin Assignments in SPI Mode

Table 9 lists the pin assignments and definitions in SPI Mode

Table 9: SPI Bus Mode Pin Definition

| Pin # | Name | Type1 | SPI Description |
|-------|----------|-------|--------------------------------|
| 1 | CS | I | Chip Select (Active low) |
| 2 | Data In | I | Host to Card Commands and Data |
| 3 | VSS1 | S | Supply Voltage Ground |
| 4 | VDD | S | Supply Voltage |
| 5 | CLK | I | Clock |
| 6 | VSS2 | S | Supply Voltage Ground |
| 7 | Data Out | O | Card to Host Data and Status |
| 8 | RSV(2) | I | Reserved |
| 9 | RSV(2) | I | Reserved |

- NOTES:
- 1) S=power supply; I=input; O=output.
 - 2) The 'RSV' pins are floating inputs. It is the responsibility of the host designer to connect external pullup resistors to those lines. Otherwise non-expected high current consumption may occur due to the floating inputs.

Each card has a set of information registers (refer to Table 10).

Table 10: SD Card Registers

| Name | Width | Description |
|------|-------|--|
| CID | 128 | Card identification number: individual card number for identification. |
| RCA1 | 16 | Relative card address: local system address of a card, dynamically suggested by the card and approved by the host during initialization. |
| CSD | 128 | Card specific data: information about the card operation conditions. |
| SCR | 64 | SD Configuration Register: information about the SD Card's special features capabilities. |
| OCR | 32 | Operation Condition Register |

NOTE: 1) The RCA register is not available in SPI Mode.

The host may reset the cards by switching the power supply off and on again. The card has its own power-on detection circuitry which puts the card into an idle state after the power-on. The card can also be reset by sending the GO_IDLE (CMD0) command.

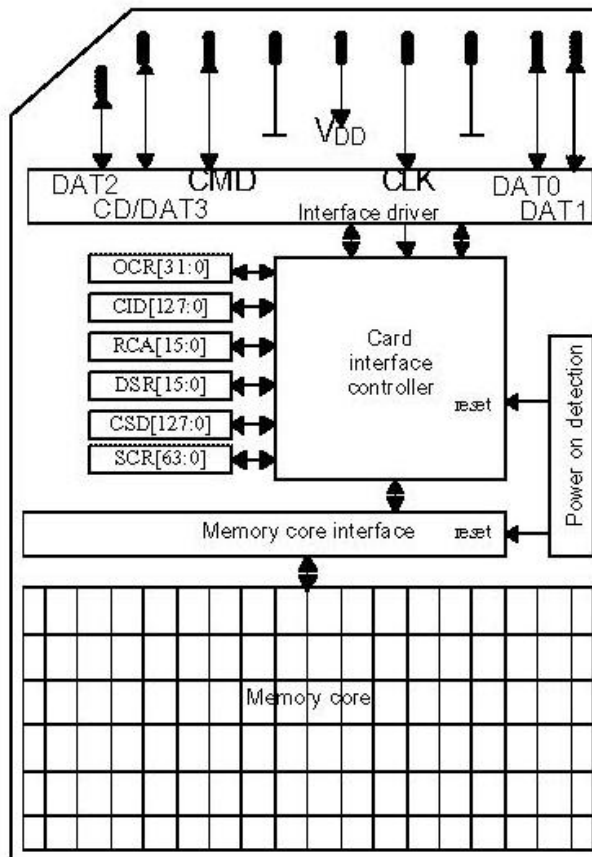


Figure 5: Industrial Grade SD Card Architecture

3.2. SD Bus Topology

The SD bus has six communication lines and three supply lines:

- **CMD**—Command is a bi-directional signal. (Host and card drivers are operating in push pull mode.)
- **DAT0-3**—Data lines are bi-directional signals. (Host and card drivers are operating in push pull mode.)
- **CLK**—Clock is a host to cards signal. (CLK operates in push pull mode.)
- **VDD**—VDD is the power supply line for all cards.
- **VSS [1:2]**—VSS are two ground lines.

Figure 6 shows the bus topology of several cards with one host in SD Bus mode.

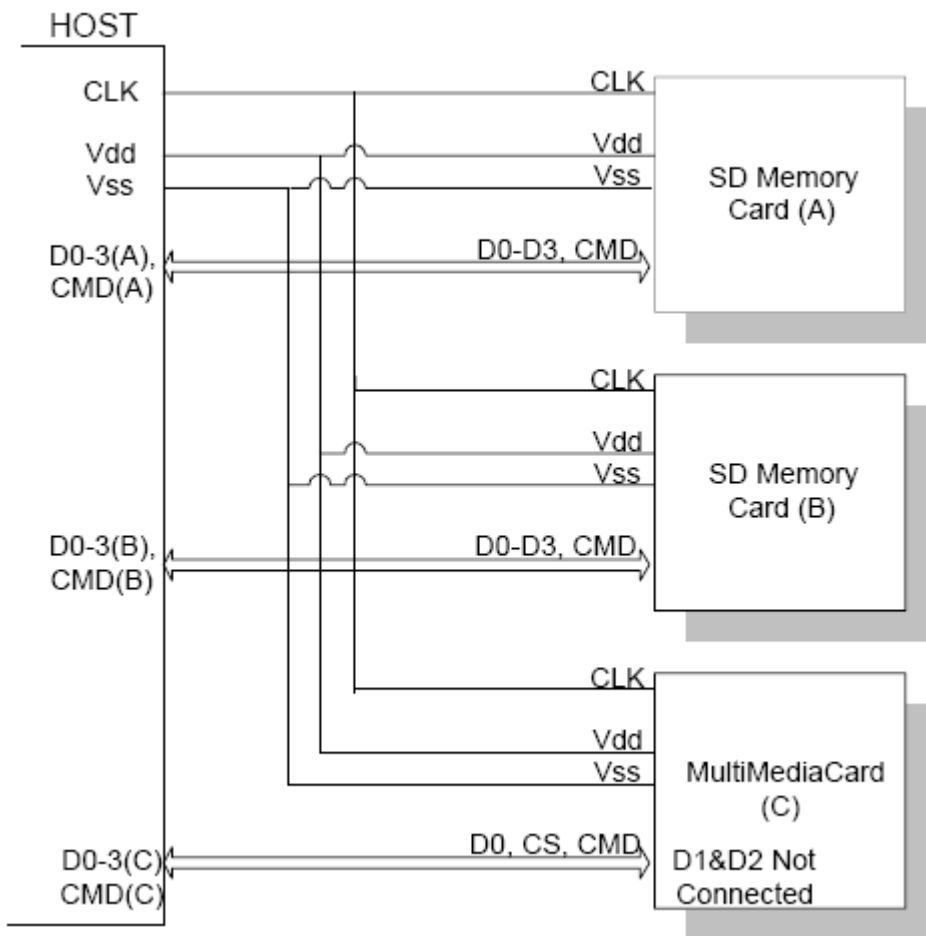


Figure 6: Industrial Grade SD Card System Bus Topology

During the initialization process, commands are sent to each card individually, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent to each card individually. However, to simplify the handling of the card stack, after initialization, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.

The SD Bus allows dynamic configuration of the number of data lines. After power-up, by default, the Industrial Grade SD Card will use only DAT0 for data transfer. After initialization, the host can change the bus width (number of active data lines). This feature allows an easy trade off between hardware cost and system performance.

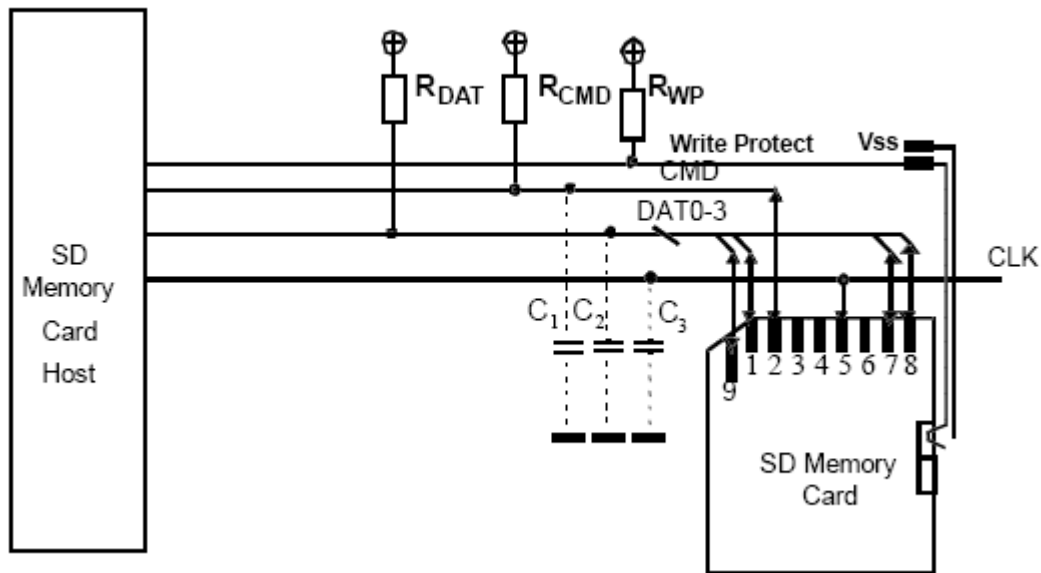


Figure 7: Bus Circuitry Diagram

R_{DAT} and R_{CMD} are pull-up resistors protecting the CMD and the DAT line against bus floating when no card is inserted or when all card drivers are in a hi-impedance mode. R_{WP} is used for the Write Protect Switch.

3.3. SPI Bus Topology

The Industrial Grade SD Card SPI interface is compatible with SPI hosts available on the market. As any other SPI device, the SD Card SPI channel consists of the following four signals:

- **CS**—Host to card Chip Select signal.
- **CLK**—Host to card clock signal.
- **Data In**—Host to card data signal.
- **Data Out**—Card to host data signal.

Another SPI common characteristic implemented in the Industrial Grade SD Card is byte transfers. All data tokens are multiples of 8-bit bytes and always byte aligned to the CS signal. The SPI standard defines the physical link only and not the complete data transfer protocol. In SPI Bus mode, the Industrial Grade SD Card uses a subset of the SD Card

protocol and command set.

The Industrial Grade SD Card identification and addressing algorithms are replaced by a hardware Chip Select (CS) signal. A card (slave) is selected, for every command, by asserting (active low) the CS signal (see Figure 8). The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception is card programming time. At this time the host can de-assert the CS signal without affecting the programming process.

The bi-directional CMD and DAT lines are replaced by uni-directional dataIn and dataOut signals. This eliminates the ability of executing commands while data is being read or written. An exception is the multi read/write operations. The Stop Transmission command can be sent during data read. In the multi block write operation a Stop Transmission token is sent as the first byte of the data block.

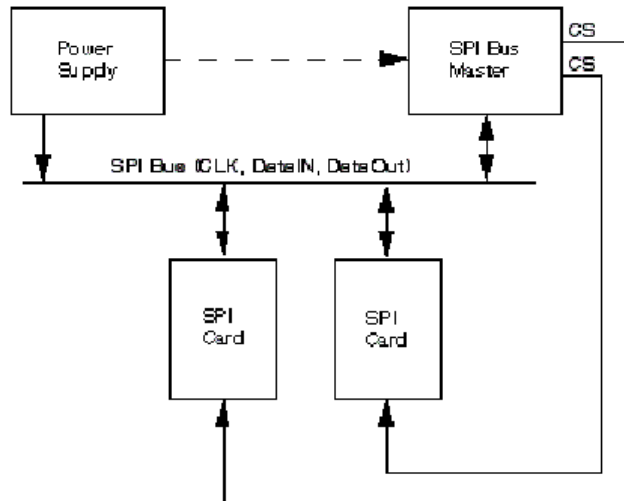


Figure 8: Industrial Grade SD Card Bus System

4. Electrical Specifications

The following tables define all DC Characteristics and AC Characteristics for the APRO Industrial Grade SD & SDHC Memory Card in THEMIS Series.

4.1. DC Character

Table 11 describes the general DC Character of APRO's Industrial Grade SD & SDHC Memory Card.

Table 11: General DC Character

| Parameter | Symbol | Min. | Max. | Unit | Note |
|-------------------------------|----------|------|------|------|------|
| Storage Temperature | Tstorage | -50 | 95 | °C | - |
| Ambient Operating Temperature | Ta | -40 | 85 | °C | - |
| 3.3V External Input Voltage | VI | -0.3 | 4.0 | V | - |

4.2. Bus Signal Line Loading

Table 12 describes Bus Signal Line Loading of APRO's Industrial Grade SD & SDHC Memory Card.

Table 12: Bus Signal Line Loading

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|--|--------|------|------|-------|-------------------------|
| Pull up resistance for SDC line | RCMD | 4.7 | 100 | K Ohm | To prevent bus floating |
| Pull up resistance for SDD line | RDAT | 50 | 100 | K Ohm | To prevent bus floating |
| Total Bus capacitance for each signal line | CL | - | 30 | pF | For single card |
| Signal Line Inductance | LL | - | 16 | nH | - |

4.3. AC Characteristics

4.3.1. Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage (see Figure 9).

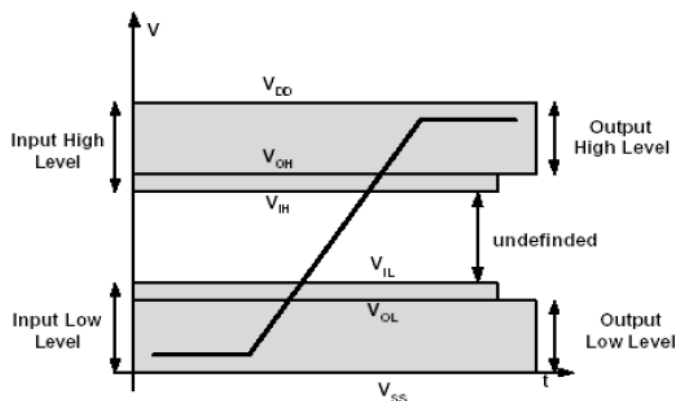


Figure 9: Bus Signal Levels

Table 13: Bus Signal Level

| Parameter | Symbol | Min. | Max. | Unit |
|---------------------|--------|------------|-----------|------|
| Input High Voltage | VIH | 0.625 x VI | VI+0.3 | V |
| Input Low Voltage | VIL | -0.3 | 0.25 x VI | V |
| Output High Voltage | VOH | 0.75 x VI | - | V |
| Output Low Voltage | VOL | - | 0.125xVI | V |
| Output High Current | IOH | -12 | - | mA |
| Output Low Current | IOL | - | 12 | mA |
| Standby Current | ISTBY | 50 | 150 | uA |

To meet the requirements of the JEDEC specification JESD8-1A, the card input and output voltages shall be within the specified ranges in Table 14 for any VDD of the allowed voltage range.

Table 14: Input and Output Voltages

| Parameter | Symbol | Min. | Max. | Unit | Conditions |
|---------------------|--------|-----------|-----------|------|--------------------------|
| Output HIGH voltage | VOH | 0.75*VDD | | V | IOH=-100µA @VDD(min.) |
| Output LOW voltage | VOL | | 0.125*VDD | V | IOL=100µA @VDD(min.) |
| Input HIGH voltage | VIH | 0.625*VDD | VDD+0.3 | V | |
| Input LOW voltage | VIL | VSS-0.3 | 0.25*VDD | V | |

4.3.2. Bus Timing (SD Default Mode)

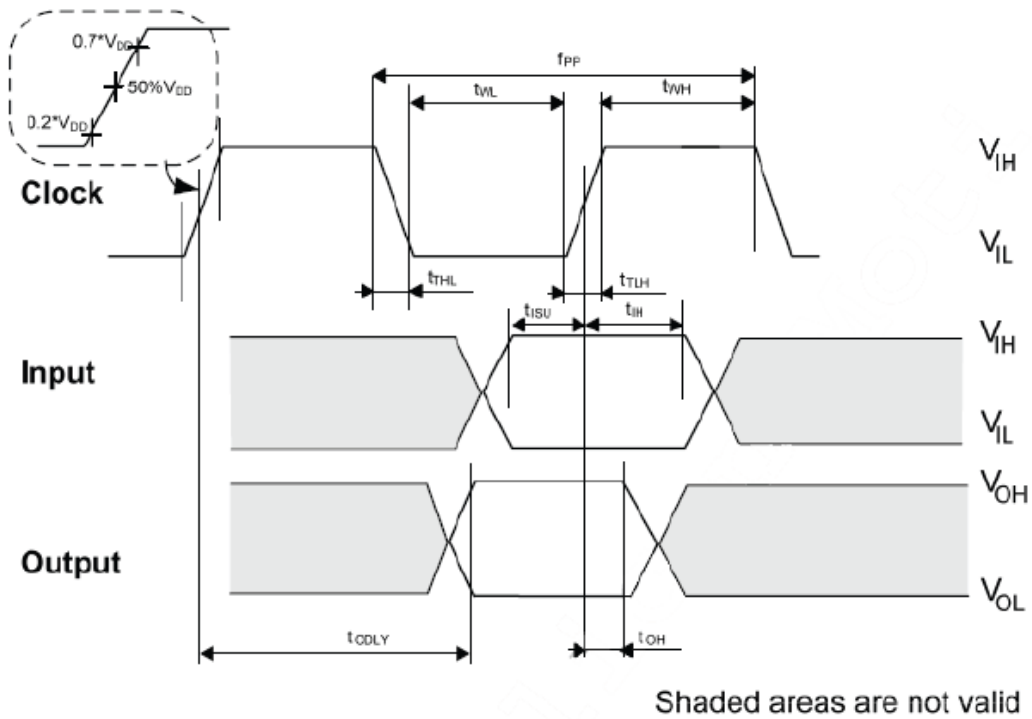


Figure 10: Timing diagram data input/output referenced to clock (High-speed)

Table 15: High-speed Mode Timing

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|-------------------------------------|------|------|------|-----------------------|
| Input SDCK | | | | | |
| Clock frequency data transfer mode | f _{PP} | 0 | 50 | MHz | CCARD ≤ 10pF (1 card) |
| Clock low time / Clock high time | t _{WL} / t _{WH} | 7 | | ns | CCARD ≤ 10pF (1 card) |
| Clock rise time / Clock fall time | t _{TLH} / t _{THL} | | 3 | ns | CCARD ≤ 10pF (1 card) |
| Input SDD/SDC, reference to SDCK | | | | | |
| Input set-up time | t _{ISU} | 6 | | ns | CCARD ≤ 10pF (1 card) |
| Input hold time | t _{IH} | 2 | | ns | CCARD ≤ 10pF (1 card) |
| Output SDD/SDC, reference to SDCK | | | | | |
| Output delay time during Data Transfer Mode | t _{ODLY} | | 14 | ns | CL ≤ 40pF (1 card) |
| Output hold time | t _{OH} | 2.5 | | ns | CL ≥ 15pF (1 card) |
| Total System capacitance for each line | CL | | 40 | pF | |

Remarks:

- (1). All timing values are measured relative to 50% of voltage level.
- (2). Rise and fall times are measured from 10% ~90% of voltage level.

4.3.3. Bus Timing (Default) – Low speed mode timing

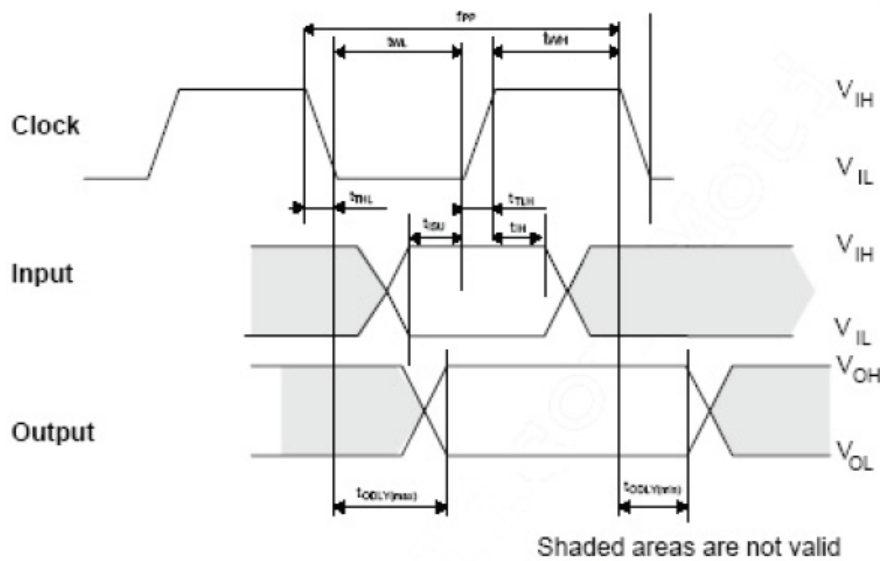


Figure 11: Timing diagram data input/output referenced to clock (Default)

Table 16: Bus timing-Parameters values (Default)

| Parameter | Symbol | Min. | Max. | Unit | Remark | |
|--|-------------------------------------|-------------------|------|------|-----------------------|--------------------|
| Input SDCK | | | | | | |
| Clock frequency data transfer mode | f _{PP} | 0 | 25 | MHz | CCARD ≤ 10pF (1 card) | |
| Clock frequency identification mode | f _{OD} | 0 | 400 | KHz | CCARD ≤ 10pF (1 card) | |
| Clock low time / Clock high time | t _{WL} / t _{WH} | 10 | | ns | CCARD ≤ 10pF (1 card) | |
| Clock rise time / Clock fall time | t _{TLH} / t _{THL} | | 10 | ns | CCARD ≤ 10pF (1 card) | |
| Input SDD/SDC, reference to SDCK | | | | | | |
| Input set-up time | t _{SU} | 5 | | ns | CCARD ≤ 10pF (1 card) | |
| Input hold time | t _{HU} | 5 | | ns | CCARD ≤ 10pF (1 card) | |
| Output SDD/SDC, reference to SDCK | | | | | | |
| Output delay time during Mode | Data Transfer | t _{ODLY} | | 14 | ns | CL ≤ 40pF (1 card) |
| Output delay time during Identification Mode | | t _{ODLY} | | 50 | ns | CL ≤ 40pF (1 card) |

Remarks:

- (1). All timing values are measured relative to 50% of voltage level.
- (2). Clock rise and fall times are measured from V_{IH} ~ V_{IL} of voltage level.

5. Register Table

Following table is the register list of SD specifications.

Table 17: Register Name v.s. SD specification

| Register Name | SD 3.0 | SD 2.0 | SD 1.1 | SD 1.01 |
|--------------------------------------|--------|--------|--------|---------|
| Operation Condition Register (OCR) | V | V | V | V |
| Card Identification Register (CID) | V | V | V | V |
| Driver Stage Register (DSR) | V | V | V | V |
| Relative Card Address Register (RCA) | V | V | V | V |
| Card Specific Data Register (CSD) | V | V | V | V |
| SD card Configuration Register (SCR) | V | V | V | V |

5.1. Operation Condition Register (OCR)

The 32-bit operation conditions register stores the VDD voltage profile of the card. In addition, this register includes status information bits. One status bit is set if the card power up procedure has been finished. This register includes another status bit indicating the card capacity status after set power up status bit. The OCR register shall be implemented by all cards. The supported voltage range is coded as shown in the following table, for High Voltage and Dual voltage SD. As long as the card is busy, the corresponding bit (31) is set to LOW. Bit 7 of OCR is newly defined for Dual Voltage Card and set to 0 in default. If a Dual Voltage Card does not receive CMD8, OCR bit 7 in the response indicates 0, and the Dual Voltage Card which received CMD8, sets the bit to 1. Additionally, this register includes 2 more status information bits. Bit 31 – Card power up status bit, this status bit is set if the card power up procedure has been finished. Bit 30 – Card capacity status bit, this status bit is set to 1 if card is High Capacity SD Memory Card. 0 indicates that the card is Standard Capacity SD Memory Card. The Card Capacity status bit is valid after the card power up procedure is completed and the card power up status bit is set to 1. The Host shall read this status bit to identify a Standard or High Capacity SD Memory Card

Table 18: OCR Table

| OCR bit | VDD voltage window | High voltage SD | Dual voltage SD |
|---------|--------------------------|-----------------|-----------------|
| [6:0] | Reserved | 000 0000 b | 000 0000 b |
| [7] | 1.7V~1.95V | 0 b | 1 b |
| [14:8] | 2.0V – 2.6V | 000 0000 b | 000 0000 b |
| [23:15] | 2.7V – 3.6V | 1 1111 1111 b | 1 1111 1111 b |
| [29:24] | Reserved | 00 0000 b | 00 0000 b |
| [30] | Card capacity status | | |
| [31] | Card power up status bit | | |

Remarks:

- (1) Pin “LVMOD” should connect to low for high voltage SD, and connect to high for dual voltage SD.
- (2) OCR bit [31] is set to LOW if the card has not finished the power up routine.
- (3) OCR bit [30] is valid only when the card power up status bit is set

5.2. Card Identification Register (CID)

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following table.

Table 19: CID Table

| CID bit | width | Name | Field |
|-----------|-------|-----------------------|-------|
| [127:120] | 8 | Manufacture ID | MID |
| [119:104] | 16 | OEM/Application ID | OID |
| [103:64] | 40 | Product Name | PNM |
| [63:56] | 8 | Product Revision | PRV |
| [55:24] | 32 | Product Serial Number | PSN |
| [23:20] | 4 | Reserved | --- |
| [19:8] | 12 | Manufacturing Date | MDT |
| [7:1] | 7 | CRC7 check sum | CRC |
| [0] | 1 | Not used, always '1' | --- |

Remarks:

(1) All content in the CID table is programmable. Manufacturer can update the CID data through ITE utility.

5.3. Driver Stage Register (DSR)

The 16-bit driver stage register is optionally used to improve the bus performance for extended operating conditions. The CSD register carries the information about the DSR register usage. This register is not implemented in SM2681BB. It is optional.

5.4. Relative Card Address Register (RCA)

The writable 16-bit relative card address register carries the card address this is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7

5.5. Card Specific Data Register (CSD)

The Card-Specific Data register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time; data transfer speed, whether the DSR register can be used etc. The programmable part of the register can be changed by CMD27.

5.6. SD 2.0 CSD for High Capacity Card Table (4GB and 8GB)

Table 20: SD 2.0 CSD for High Capacity Card Table (4GB and 8GB)

| CSD bit | Width | Name | Field | Value | Note |
|-----------|-------|------------------------------|----------------------|---------|------------------|
| [127:126] | 2 | CSD structure | CSD_STRUCTURE | 01 b | v2.0 (>2GB card) |
| [125:120] | 6 | Reserved | --- | --- | --- |
| [119:112] | 8 | Data read access-time 1 | (TAAC) | 0E h | 1 ms (*3) |
| [111:104] | 8 | Data read access-time 2 | (NSAC) | 00 h | (*3) |
| [103:96] | 8 | Max. data transfer rate | (TRAN_SPEED) | 32 h | 25 MHz |
| [95:84] | 12 | Card command classes | CCC | 5F5 h | (*1) |
| [83:80] | 4 | Max. read data block length | (READ_BLK_LEN) | 9 h | 512 bytes(*3) |
| [79] | 1 | Partial block read allowed | (READ_BLK_PARTIAL) | 0 b | Not Support(*3) |
| [78] | 1 | Write block misalignment | (WRITE_BLK_MISALIGN) | 0 b | Not Support(*3) |
| [77] | 1 | Read block misalignment | (READ_BLK_MISALIGN) | 0 b | Not Support(*3) |
| [76] | 1 | DSR implemented | DSR_IMP | 0 b | Not support |
| [75:70] | 6 | Reserved | --- | 000000b | --- |
| [69:48] | 22 | Device size | C_SIZE | (*2) | (*2) |
| [47] | 1 | Reserved | --- | 0 | --- |
| [46] | 1 | Erase single block enable | (ERASE_BLK_EN) | 1 b | allowed(*3) |
| [45:39] | 7 | Erase sector size | (SECTOR_SIZE) | 7Fh | 64KB(*3) |
| [38:32] | 7 | Write protect group size | (WP_GRP_SIZE) | 00h | (*3) |
| [31] | 1 | Write protect group enable | (WP_GRP_ENABLE) | 0 b | Not Support(*3) |
| [30:29] | 2 | Reserved | --- | --- | --- |
| [28:26] | 3 | Write speed factor | (R2W_FACTOR) | 010 b | 4X(*3) |
| [25:22] | 4 | Max. write data block length | (WRITE_BLK_LEN) | 9 h | 512 bytes(*3) |
| [21] | 1 | Partial block write allowed | (WRITE_BLK_PARTIAL) | 0 b | Not Support(*3) |
| [20:16] | 5 | Reserved | --- | --- | --- |
| [15] | 1 | File format group | (FILE_FORMAT_GRP) | 0 b | HD like FAT(*3) |
| [14] | 1 | Copy flag | COPY | 0 b | Not copied |
| [13] | 1 | Permanent write protection | PERM_WRITE_PROTECT | 0 b | Not protected |
| [12] | 1 | Temporary write protection | TMP_WRITE_PROTECT | 0 b | Not protected |
| [11:10] | 2 | File format | (FILE_FORMAT) | 00 b | HD like FAT(*3) |
| [9:8] | 2 | ECC code | ECC | 00 b | None |
| [7:1] | 7 | CRC | CRC | --- | --- |
| [0] | 1 | Not used, always '1' | --- | 1 b | --- |

Remarks:

(1) Support command class 0, 2, 4,5,6,7,8,10. Include: Basic, Block read/write, Erase, Write protection, application command, Lock card and switch function. Not support 1, 3. Include: Stream read/write.

(2)~ 4) This field is not a constant value. The value will be changed by different flash memory. For example, the value of Samsung SLC flash is different from Toshiba MLC flash.

(*3) The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enable host, which refers to these fields, to keep compatibility to CSD Version 1.0.

Note: bit [15:0] is programmable by host side. Please reference to SD specification for detail information.

5.7. SD 2.0 CSD for Standard Capacity Card Table (128MB to 2GB)

Table 21: SD 2.0 CSD for High Capacity Card Table (128MB and 2GB)

| CSD bit | Width | Name | Field | Value | Note |
|-----------|-------|------------------------------|--------------------|-------|-----------------------------|
| [127:126] | 2 | CSD structure | CSD_STRUCTURE | 00 b | v1.0-v1.1 v2.0 (<=2GB card) |
| [125:120] | 6 | Reserved | --- | --- | --- |
| [119:112] | 8 | Data read access-time 1 | TAAC | 7F h | 80 ms |
| [111:104] | 8 | Data read access-time 2 | NSAC | FF h | 25.5k clocks |
| [103:96] | 8 | Max. data transfer rate | TRAN_SPEED | 32 h | 25 MHz |
| [95:84] | 12 | Card command classes | CCC | 5F5 h | (*1) |
| [83:80] | 4 | Max. read data block length | READ_BL_LEN | 9 h | 512 bytes |
| [79] | 1 | Partial block read allowed | READ_BLK_PARTIAL | 1 b | Support |
| [78] | 1 | Write block misalignment | WRITE_BLK_MISALIGN | 1 b | Support |
| [77] | 1 | Read block misalignment | READ_BLK_MISALIGN | 1 b | Support |
| [76] | 1 | DSR implemented | DSR_IMP | 0 b | Not support |
| [75:74] | 2 | Reserved | --- | --- | --- |
| [73:62] | 12 | Device size | C_SIZE | (*2) | (*2) |
| [61:59] | 3 | Max. R_curr @ VDD min | VDD_R_CURR_MIN | 101 b | 35 mA |
| [58:56] | 3 | Max R_curr @ VDD max | VDD_R_CURR_MAX | 101 b | 45 mA |
| [55:53] | 3 | Max W_curr @ VDD min | VDD_W_CURR_MIN | 101 b | 35 mA |
| [52:50] | 3 | Max W_curr @ VDD max | VDD_W_CURR_MAX | 101 b | 45 mA |
| [49:47] | 3 | Device size multiplier | C_SIZE_MULT | (*2) | (*2) |
| [46] | 1 | Erase single block enable | ERASE_BLK_EN | 0 b | Not allowed |
| [45:39] | 7 | Erase sector size | SECTOR_SIZE | (*3) | (*3) |
| [38:32] | 7 | Write protect group size | WP_GRP_SIZE | (*4) | (*4) |
| [31] | 1 | Write protect group enable | WP_GRP_ENABLE | 1 b | Support |
| [30:29] | 2 | Reserved | --- | --- | --- |
| [28:26] | 3 | Write speed factor | R2W_FACTOR | 101 b | 32X |
| [25:22] | 4 | Max. write data block length | WRITE_BL_LEN | 9 h | 512 bytes |
| [21] | 1 | Partial block write allowed | WRITE_BLK_PARTIAL | 1 b | Support |
| [20:16] | 5 | Reserved | --- | --- | --- |
| [15] | 1 | File format group | FILE_FORMAT_GRP | 0 b | HD like FAT |
| [14] | 1 | Copy flag | COPY | 0 b | Not copied |
| [13] | 1 | Permanent write protection | PERM_WRITE_PROTECT | 0 b | Not protected |
| [12] | 1 | Temporary write protection | TMP_WRITE_PROTECT | 0 b | Not protected |
| [11:10] | 2 | File format | FILE_FORMAT | 00 b | HD like FAT |
| [9:8] | 2 | ECC code | ECC | 00 b | None |
| [7:1] | 7 | CRC | CRC | --- | --- |
| [0] | 1 | Not used, always '1' | --- | 1 b | --- |

Remarks:

(1) Support command class 0, 2, 4,5,6,7,8,10. Include: Basic, Block read/write, Erase, Write protection, application command, Lock card and switch function. Not support 1, 3. Include: Stream read/write.

(2)- (4) This field is not a constant value. The value will be changed by different flash memory. For example, the value of Samsung SLC flash is different from Toshiba MLC flash.

Note: bit [15:0] is programmable by host side. Please reference to SD specification for detail information.

5.8. SD 1.1 CSD Table

Table 22: SD 1.1 CSD Table

| CSD bit | Width | Name | Field | Value | Note |
|-----------|-------|------------------------------|--------------------|-------|---------------|
| [127:126] | 2 | CSD structure | CSD_STRUCTURE | 00 b | v1.0-v1.1 |
| [125:120] | 6 | Reserved | --- | --- | --- |
| [119:112] | 8 | Data read access-time 1 | TAAC | 7F h | 80 ms |
| [111:104] | 8 | Data read access-time 2 | NSAC | FF h | 25.5k clocks |
| [103:96] | 8 | Max. data transfer rate | TRAN_SPEED | 32 h | 25 MHz |
| [95:84] | 12 | Card command classes | CCC | 5F5 h | (*1) |
| [83:80] | 4 | Max. read data block length | READ_BL_LEN | 9 h | 512 bytes |
| [79] | 1 | Partial block read allowed | READ_BL_PARTIAL | 1 b | Support |
| [78] | 1 | Write block misalignment | WRITE_BLK_MISALIGN | 1 b | Support |
| [77] | 1 | Read block misalignment | READ_BLK_MISALIGN | 1 b | Support |
| [76] | 1 | DSR implemented | DSR_IMP | 0 b | Not support |
| [75:74] | 2 | Reserved | --- | --- | --- |
| [73:62] | 12 | Device size | C_SIZE | (*2) | (*2) |
| [61:59] | 3 | Max. R_curr @ VDD min | VDD_R_CURR_MIN | 101 b | 35 mA |
| [58:56] | 3 | Max R_curr @ VDD max | VDD_R_CURR_MAX | 101 b | 45 mA |
| [55:53] | 3 | Max W_curr @ VDD min | VDD_W_CURR_MIN | 101 b | 35 mA |
| [52:50] | 3 | Max W_curr @ VDD max | VDD_W_CURR_MAX | 101 b | 45 mA |
| [49:47] | 3 | Device size multiplier | C_SIZE_MULT | (*2) | (*2) |
| [46] | 1 | Erase single block enable | ERASE_BLK_EN | 0 b | Not allowed |
| [45:39] | 7 | Erase sector size | SECTOR_SIZE | (*3) | (*3) |
| [38:32] | 7 | Write protect group size | WP_GRP_SIZE | (*4) | (*4) |
| [31] | 1 | Write protect group enable | WP_GRP_ENABLE | 1 b | Support |
| [30:29] | 2 | Reserved | --- | --- | --- |
| [28:26] | 3 | Write speed factor | R2W_FACTOR | 101 b | 32X |
| [25:22] | 4 | Max. write data block length | WRITE_BL_LEN | 9 h | 512 bytes |
| [21] | 1 | Partial block write allowed | WRITE_BL_PARTIAL | 1 b | Support |
| [20:16] | 5 | Reserved | --- | --- | --- |
| [15] | 1 | File format group | FILE_FORMAT_GRP | 0 b | HD like FAT |
| [14] | 1 | Copy flag | COPY | 0 b | Not copied |
| [13] | 1 | Permanent write protection | PERM_WRITE_PROTECT | 0 b | Not protected |
| [12] | 1 | Temporary write protection | TMP_WRITE_PROTECT | 0 b | Not protected |
| [11:10] | 2 | File format | FILE_FORMAT | 00 b | HD like FAT |
| [9:8] | 2 | ECC code | ECC | 00 b | None |
| [7:1] | 7 | CRC | CRC | --- | --- |
| [0] | 1 | Not used, always '1' | --- | 1 b | --- |

Remarks:

(1) Support command class 0, 2, 4,5,6,7,8,10, including: Basic, Block read/write, Erase, Write protection, application command, Lock card and switch function.

(2)~ (4) This field is not a constant value. The value will be changed by different flash memory. For example, the value of Samsung SLC flash is different from Toshiba MLC flash.

Note: bit [15:0] is programmable by host side. Please reference to SD specification for detail information.

5.9. SD 1.01 CSD Table

Table 23: SD 1.01 CSD Table

| CSD bit | Width | Name | Field | Value | Note |
|-----------|-------|------------------------------|--------------------|-------|---------------|
| [127:126] | 2 | CSD structure | CSD_STRUCTURE | 00 b | v1.0 |
| [125:120] | 6 | Reserved | --- | --- | --- |
| [119:112] | 8 | Data read access-time 1 | TAAC | 7F h | 80 ms |
| [111:104] | 8 | Data read access-time 2 | NSAC | FF h | 25.5k clocks |
| [103:96] | 8 | Max. data transfer rate | TRAN_SPEED | 32 h | 25 MHz |
| [95:84] | 12 | Card command classes | CCC | 1F5 h | (*1) |
| [83:80] | 4 | Max. read data block length | READ_BL_LEN | 9 h | 512 bytes |
| [79] | 1 | Partial block read allowed | READ_BL_PARTIAL | 1 b | Support |
| [78] | 1 | Write block misalignment | WRITE_BLK_MISALIGN | 1 b | Support |
| [77] | 1 | Read block misalignment | READ_BLK_MISALIGN | 1 b | Support |
| [76] | 1 | DSR implemented | DSR_IMP | 0 b | Not support |
| [75:74] | 2 | Reserved | --- | --- | --- |
| [73:62] | 12 | Device size | C_SIZE | (*2) | (*2) |
| [61:59] | 3 | Max. R_curr @ VDD min | VDD_R_CURR_MIN | 101 b | 35 mA |
| [58:56] | 3 | Max R_curr @ VDD max | VDD_R_CURR_MAX | 101 b | 45 mA |
| [55:53] | 3 | Max W_curr @ VDD min | VDD_W_CURR_MIN | 101 b | 35 mA |
| [52:50] | 3 | Max W_curr @ VDD max | VDD_W_CURR_MAX | 101 b | 45 mA |
| [49:47] | 3 | Device size multiplier | C_SIZE_MULT | (*2) | (*2) |
| [46] | 1 | Erase single block enable | ERASE_BLK_EN | 0 b | Not allowed |
| [45:39] | 7 | Erase sector size | SECTOR_SIZE | (*3) | (*3) |
| [38:32] | 7 | Write protect group size | WP_GRP_SIZE | (*4) | (*4) |
| [31] | 1 | Write protect group enable | WP_GRP_ENABLE | 1 b | Support |
| [30:29] | 2 | Reserved | --- | --- | --- |
| [28:26] | 3 | Write speed factor | R2W_FACTOR | 101 b | 32X |
| [25:22] | 4 | Max. write data block length | WRITE_BL_LEN | 9 h | 512 bytes |
| [21] | 1 | Partial block write allowed | WRITE_BL_PARTIAL | 1 b | Support |
| [20:16] | 5 | Reserved | --- | --- | --- |
| [15] | 1 | File format group | FILE_FORMAT_GRP | 0 b | HD like FAT |
| [14] | 1 | Copy flag | COPY | 0 b | Not copied |
| [13] | 1 | Permanent write protection | PERM_WRITE_PROTECT | 0 b | Not protected |
| [12] | 1 | Temporary write protection | TMP_WRITE_PROTECT | 0 b | Not protected |
| [11:10] | 2 | File format | FILE_FORMAT | 00 b | HD like FAT |
| [9:8] | 2 | ECC code | ECC | 00 b | None |
| [7:1] | 7 | CRC | CRC | --- | --- |
| [0] | 1 | Not used, always '1' | --- | 1 b | --- |

Remarks:

(1) Support command class 0,2,4,5,6,7,8. Include: Basic, Block read/write, Erase, Write protection, application command, and Lock card.

(2)~ (4) This field is not a constant value. The value will be changed by different flash memory. For example, the value of Samsung SLC flash is different from Toshiba MLC flash.

Note: bit [15:0] is programmable by host side. Please reference to SD specification for detail information.

5.10. SD Card Configuration Register (SCR)

The CSD register is another configuration register in SD card. SCR provides on SD card's special features that were configured into the given card. The size of SCR is 64 bit.

SCR is a read only register.

Table 24: SCR Table

| SCR bit | Width | Name | Field | Value | Note |
|---------|-------|-------------------------|-----------------------|--------|---------------------|
| [63:60] | 4 | SCR structure | SCR_STRUCTURE | 0000 b | v1.0-vv2.0 |
| [59:56] | 4 | SD card spec. version | SD_SPEC | 0010 b | V2.0 |
| [55] | 1 | Data status after erase | DATA_STAT_AFTER_ERASE | 0 b | Zero after erase |
| [54:52] | 3 | SD security support | SD_SECURITY | 011 b | Secure-protocol 2.0 |
| [51:48] | 4 | DAT bus width support | SD_BUS_WIDTH | 0101 b | Support 1/4 bit |
| [47:32] | 16 | Reserved | --- | --- | --- |
| [31:0] | 32 | Reserved | --- | --- | --- |

6. SD & SDHC Memory Card Protocol Description

6.1. SD Bus Protocol

Communication over the SD bus is based on command and data bit streams, which are initiated by a start bit and terminated, by a stop bit:

- **Command** — A command is a token that starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- **Response** — A response is a token that is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- **Data** — Data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

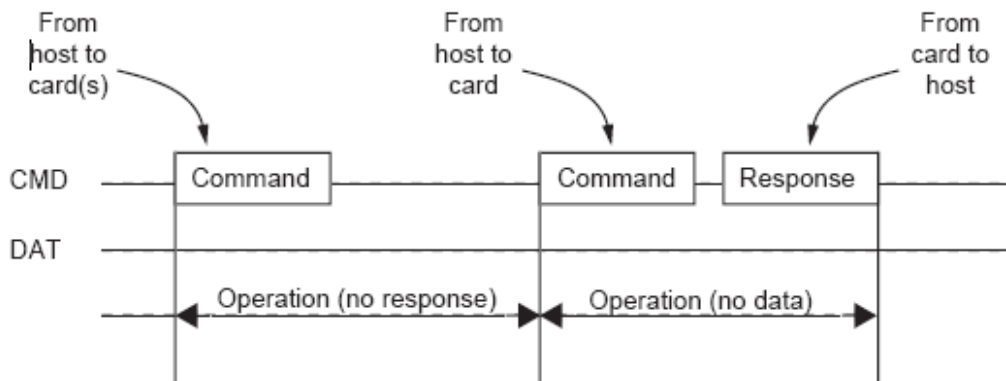


Figure 12: “No Response” and “No Data” Operations

Card addressing is implemented using a session address that is assigned to the card during the initialization phase. The basic transaction on the SD bus is the command/response transaction (see Figure 13). This type of bus transaction transfers their information directly within the command or response structure. In addition, some operations have a data token.

Data transfers to/from the Industrial Grade SD Card are done in blocks. Data blocks are always followed by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode is better for faster write operation. A multiple block transmission is terminated when a stop command follows on the CMD line. Data transfer can be configured by the host to use single or multiple data lines (as long as the card supports this feature).

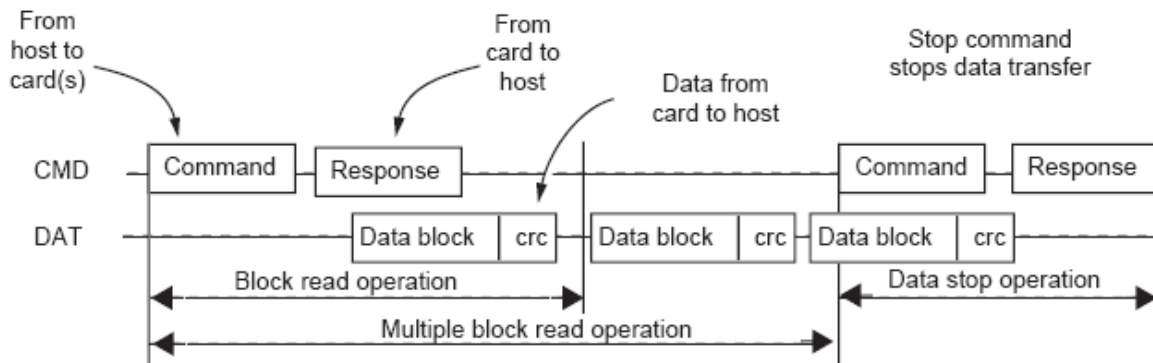


Figure 13: Multiple Block Read Operation

The block write operation uses a simple busy signaling of the write operation duration on the DAT0 data line (see Figure 14) regardless of the number of data lines used for transferring the data.

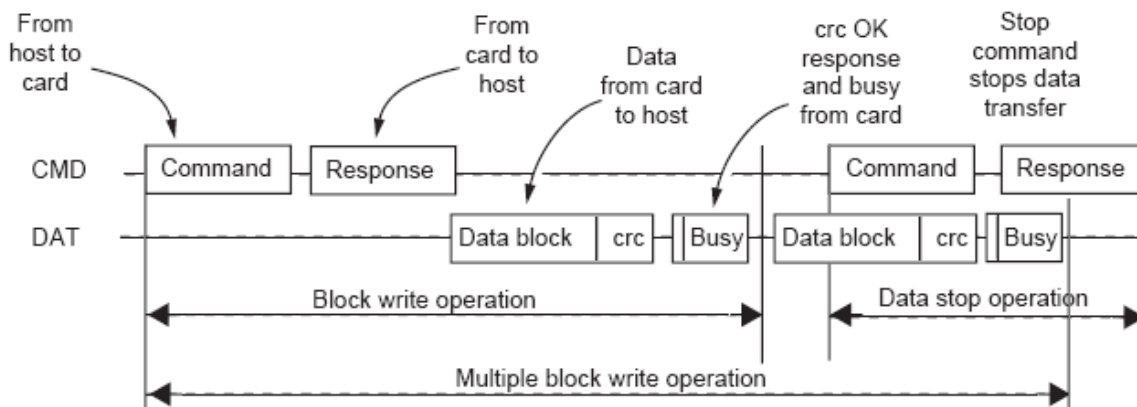


Figure 14: Multiple Block Write Operation

Command tokens have the coding scheme shown in Figure 15.

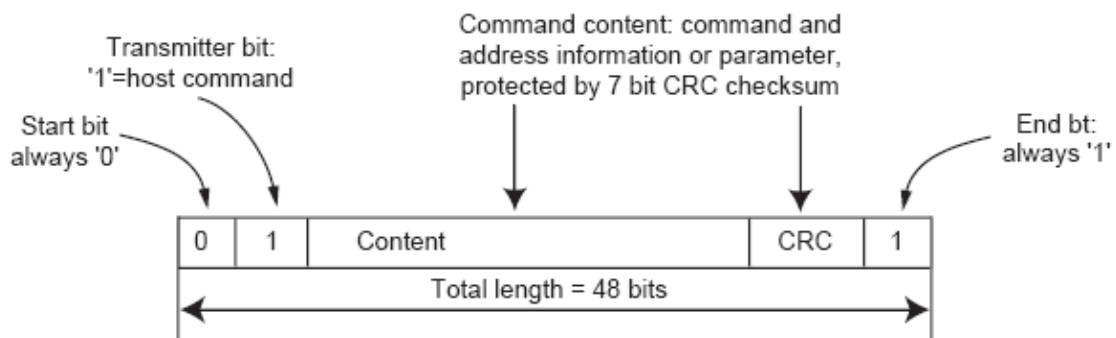


Figure 15: Command Token Format

Each command token is preceded by a start bit ('0') and succeeded by an end bit ('1'). The total length is 48 bits. Each token is protected by CRC bits so that transmission errors can be detected and the operation may be repeated. Response tokens have four coding schemes depending on their content. The token length is either 48 or 136 bits. The CRC protection algorithm for block data is a 16-bit CCITT polynomial.

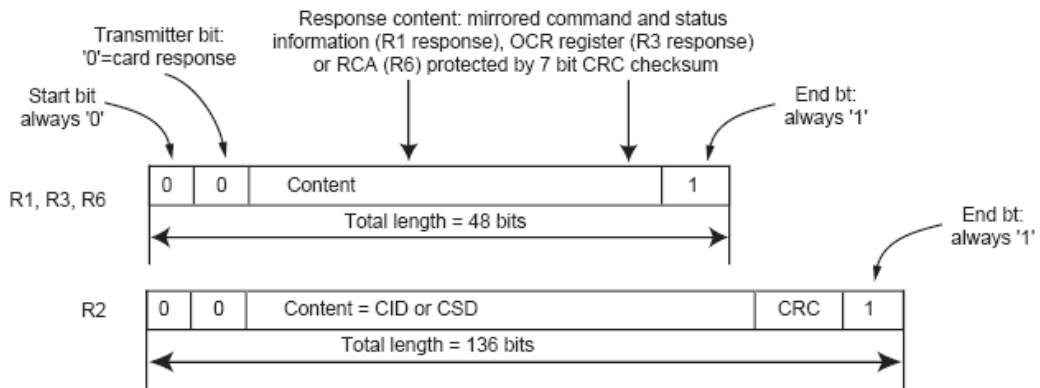


Figure 16: Response Token Format

In the CMD line, the MSB bit is transmitted first, whereas the LSB bit is transmitted last.

When the wide bus option is used, the data is transferred 4 bits at a time (see Figure 17). Start and end bits, as well as the CRC bits, are transmitted for every one of the DAT lines. CRC bits are calculated and checked for every DAT line individually. The CRC status response and Busy indication will be sent by the card to the host on DAT0 only (DAT1-DAT3 during that period are “don’t care”).

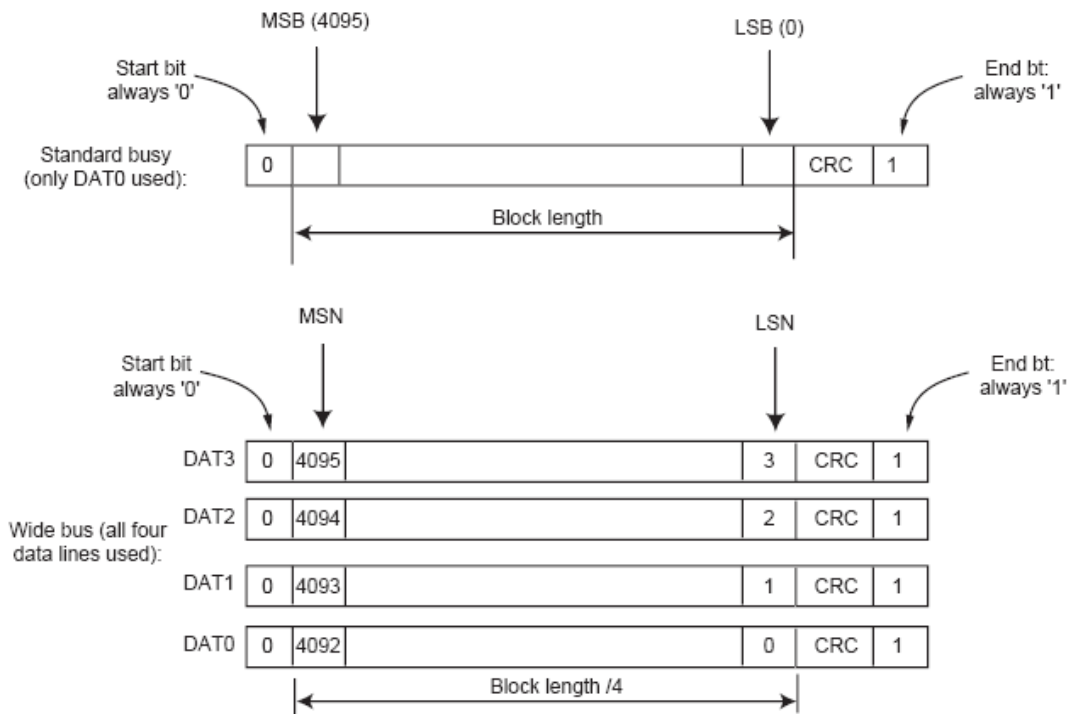


Figure 17: Data Packet Format

7. SPI Protocol Definition

7.1. SPI Bus Protocol

While the Industrial Grade SD Card channel is based on command and data bit-streams, which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of eight bit bytes and is byte aligned (multiples of eight clocks) to the CS signal.

Similar to the SD Bus protocol, the SPI messages are built from command, response and data-block tokens. All communication between host and cards is controlled by the host (master). The host starts every bus transaction by asserting the CS signal low.

The response behavior in SPI Bus mode differs from the SD Bus mode in the following three ways:

- The selected card always responds to the command.
- An eight or 16-bit response structure is used.
- When the card encounters a data retrieval problem, it will respond with an error response (which replaces the expected data block) rather than time-out as in the SD Bus mode.

In addition to the command response, every data block sent to the card during write operations will be responded with a special data response token. A data block may be as big as one card write block (WRITE_BL_LEN) and as small as a single byte.¹

Note : 1) The default block length is as specified in the CSD (512 bytes). A set block length of less than 512 bytes will cause a write error. The only valid write set block length is 512 bytes. CMD16 is not mandatory if the default is accepted.

7.1.1. Data Read

SPI mode supports single block and multiple block read operations (SD Card CMD17 or CMD18). Upon reception of a valid read command the card will respond with a response token followed by a data token in the length defined in a previous SET_BLOCK_LENGTH (CMD16) command (see Figure 18).

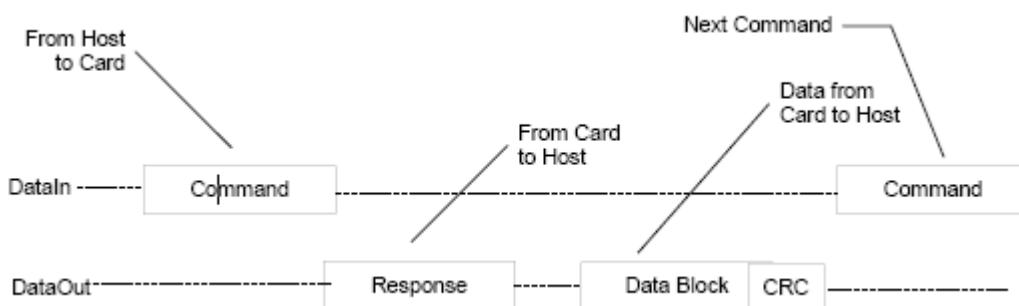


Figure 18: Single Block Read Operation

A valid data block is suffixed with a 16-bit CRC generated by the standard CCITT polynomial:

$$x^{16}+x^{12}+x^5+1.$$

The maximum block length is 512 bytes as defined by READ_BL_LEN (CSD parameter). Block lengths can be any number between 1 and READ_BL_LEN.

The start address can be any byte address in the valid address range of the card. Every block, however, must be contained in a single physical card sector.

In case of data retrieval error, the card will not transmit any data. Instead, a special data error token will be sent to the host. Figure 19 shows a data read operation, which terminated with an error token rather than a data block.

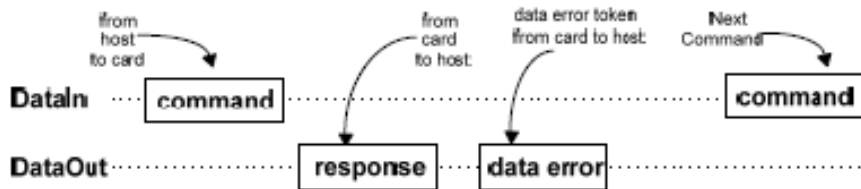


Figure 19: Read Operation—Data Error

In the case of a Multiple Block Read operation, every transferred block has a 16-bit CRC suffix. The Stop Transmission command (CMD12) will actually stop the data transfer operation (the same as in SD Bus mode).

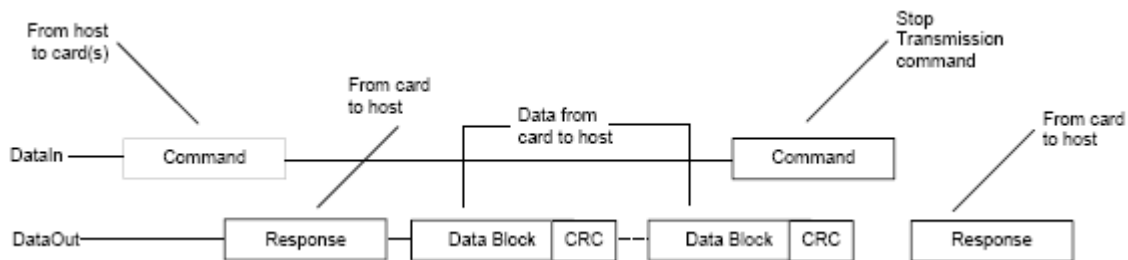


Figure 20: Multiple Block Read Operation

7.1.2. Data Write

In SPI mode, the Industrial Grade SD Card supports single block or multiple block write operations. Upon reception of a valid write command (SD Card CMD24 or CMD25), the card will respond with a response token and will wait for a data block to be sent from the host. CRC suffix and start address restrictions are identical to the read operation (see Figure 21). The only valid block length, however, is 512 bytes. Setting a smaller block length will cause a write error on the next write command.

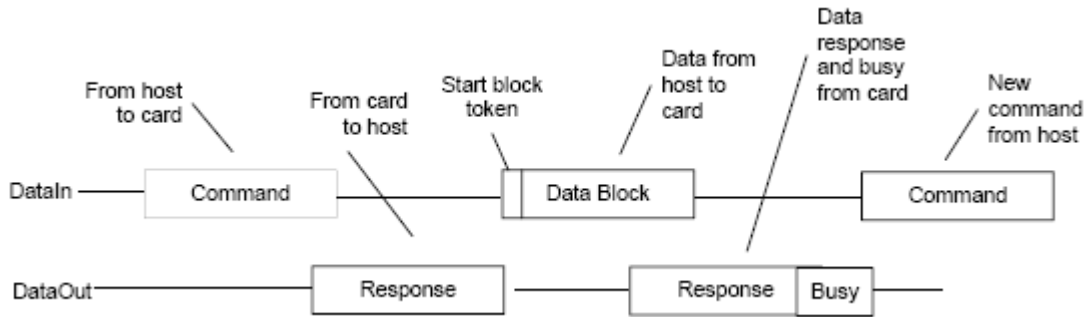


Figure 21: Single Block Write Operation

Every data block has a prefix or 'start block' token (one byte). After a data block is received the card will respond with a data-response token, and if the data block is received with no errors, it will be programmed. As long as the card is busy programming, a continuous stream of busy tokens will be sent to the host (effectively holding the dataOut line low).

Once the programming operation is completed, the host must check the results of the programming using the SEND_STATUS command (CMD13). Some errors (e.g., address out of range, write protect violation, etc.) are detected during programming only. The only validation check performed on the data block and communicated to the host via the data-response token is CRC and general Write Error indication.

In Multiple Block write operation the stop transmission will be done by sending 'Stop Tran' token instead of 'Start Block' token at the beginning of the next block. In case of Write Error indication (on the data response) the host shall use SEND_NUM_WR_BLOCKS (ACMD22) in order to get the number of well written write blocks

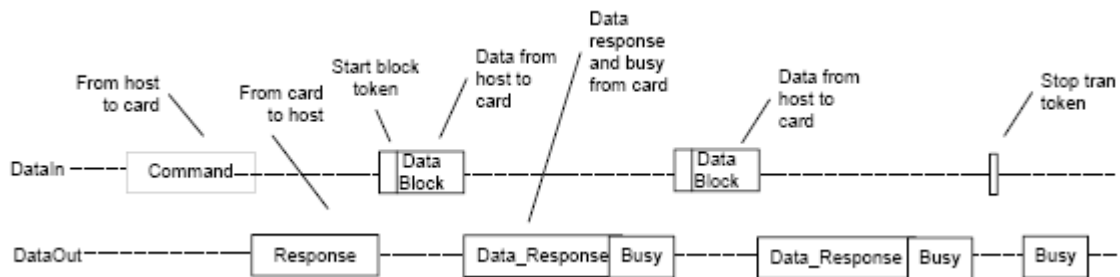



Figure 22: Multiple Block Write Operation


Resetting the CS signal while the card is busy does not terminate the programming process. The card releases the dataOut line (tristate) and continues to program. If the card is reselected before the programming is done, the dataOut line will be forced back to low and all commands will be rejected.

Resetting a card (using CMD0) will terminate any pending or active programming operation. This may destroy the data formats on the card. It is the host's responsibility to prevent it.

Appendix A. Ordering Information

Part Number List:

| Industrial SD Memory Card | | |
|---|----------|-------------------------|
| Product Picture | Capacity | -40° C~ +85° C |
|  | 128MB | WPSDC128M-EAISI-16(-32) |
| | 256MB | WPSDC256M-EAISI-16(-32) |
| | 512MB | WPSDC512M-EAISI-16(-32) |
| | 1GB | WPSDC001G-EAISI-16(-32) |
| | 2GB | WPSDC002G-EAISI-16(-32) |

| Industrial Secure Digital High Capacity (SDHC) Memory Card | | |
|---|----------|--------------------|
| Product Picture | Capacity | -40° C~ +85° C |
|  | 4GB | WPSDH004G-EAISI-32 |
| | 8GB | WPSDH008G-EAISI-32 |
| Remark: The default setting of file allocation table for flash storage are: 128MB ~ 2GB: FAT16 / 4GB, 8GB: FAT32(Do not support FAT16) FAT type setting based on ATA/ATAPI specification. | | |

Part number decoder :

X1 X2 X3 X4 X5 X6 X7 X8 X9 — **X11 X12 X13 X14 X15** — **X17 X18**

X1 : Grade

W : Industrial grade – operating temp. -40° C ~ +85 ° C

X2 : The material of case

P : Plastic casing

X3 X4 X5 : Product category

SDC : SD & SDHC memory card

SDH : Secure Digital High Capacity (SDHC) memory card

X6 X7 X8 X9 : Capacity

128M: 128MB **002G:** 2GB

256M: 256MB **004G:** 4GB

512M: 512MB **008G:** 8GB

001G: 1GB

X11 : Controller

E : ITE Controller

X12 : Controller version

A, B, C.....

X13 : Controller grade

I : Industrial grade

X14 : Flash IC

S : Samsung SLC-NAND Flash IC

X15 : Flash IC grade / Type

I : Industrial grade

X17 X18 : File allocation table

16: FAT16

32: FAT32

Appendix B. Limited Warranty

APRO warrants your Industrial SD & SDHC Memory Cards against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO .

Product shall be returned to with shipping prepaid. If the product fails to conform based on customers' purchasing orders, will reimburse customers for the transportation charges incurred.

Warranty Period:

| | |
|------------------------|----------------|
| WPSDCxxxG-EAISI | 5 years |
| WPSDHxxxG-EAISI | 5 years |



The warranty period is able to extend. Please contact APRO or Your APRO distributors for more information.