APRO Co., Ltd.

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Product Specification

MLC micro SATA II Flash (MSF) Module

-HERMES-D Series-

Doc-No: 100-SPMSF-JDML-1V0

Revision History

Revision	***Description***	***Date***
01V0	*Initial Released*	*2012/8/08*

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1. Introduction

APRO MLC micro SATA II Flash Module – HERMES-D Series is an extremely compact design with high performance for SATA interfaces which follows Serial ATA 2.6 (3.0Gbps) and compatible with ATAPI-7 specifications. It is mainly used Micron NAND Type MLC Flash memory chips managed by serial ATA controller. The sequential read is up to 124.0 MB/sec, and sequential write up to 73.0 MB/sec.

The APRO MLC micro SATA II Flash Module – HERMES-D Series products provide a high level interface to the host computer. This interface allows a host computer to issue commands to the Flash Module to read or write blocks of memory, and the host addresses the card in 512 byte sectors. Each sector is protected by a powerful 16 bits Error Correcting Code (ECC).

The power operating voltage supports 5V. Particularly it is built-in power pin as the 7th pin of 7pin header (w/fuse) or power input power cable (w/o fuse). They are ideal high performance of Flash storages for applications such like Digital Signage, Multimedia Car PC, Terminal Information Systems, Medical Equipments, Telecommunication and Enterprises Systems.

Figure 1 shows a block diagram of the used high tech Mini SATA Module controller.

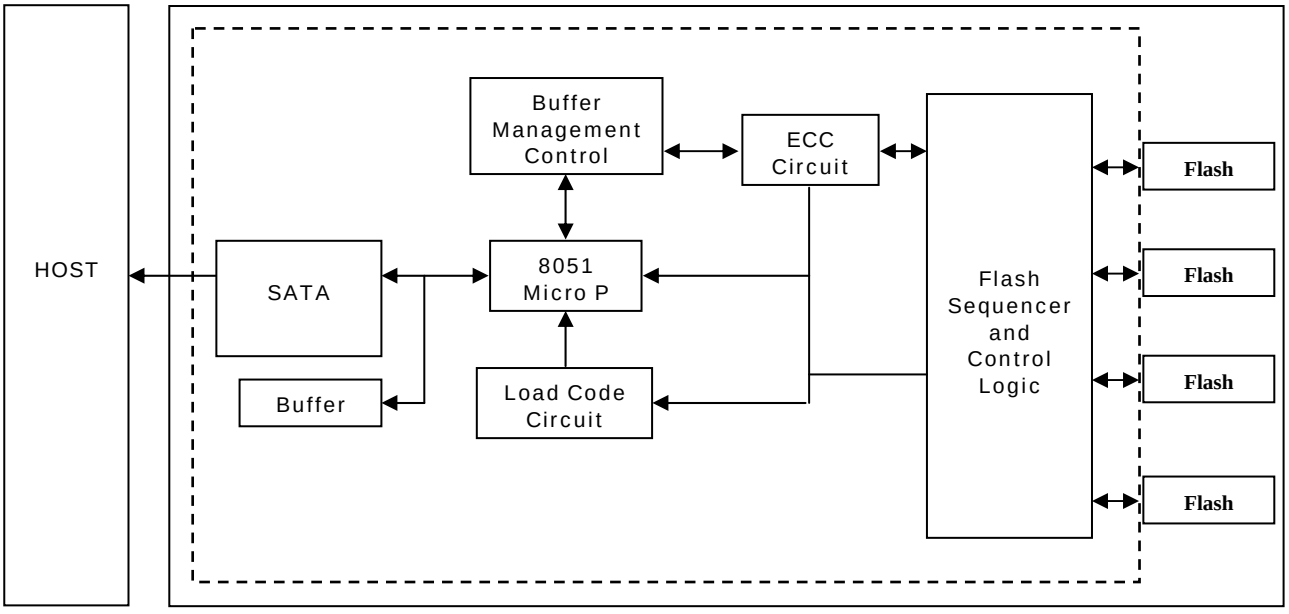

Figure 1: MLC micro SATA II Flash Module – HERMES-D Series controller block diagram

1.1. Scope

This document describes the features and specifications of APRO MLC micro SATA II Flash (MSF) Module – HERMES-D Series. In the appendix, there provides order information for the most convenient reference.

1.2. System Features

- MLC-NAND type flash technology
- Capacity from 4GB up to 128GB (Quad channel)
- Standard 7 pins SATA female connector

- SATA 1.0a and SATA 2.6 specification compliance
- Performance up to 124.0 MB/sec (Quad channel)
- Supports SATA I/II (1.5/3.0Gbps) interface
- Supports write protect function by switch
- Supports BCH ECC 16 bits per 512 bytes
- +5 V ±10%, optional Built-in power pin as the 7th pin of 7 pin header (w/fuse) or power input power cable (w/o fuse).
- MTBF > 4,000,000 hours.
- Endurance cycles greater than 2,000,000 cycles
- Vibration : 15 G, compliance to MIL-STD-810F
- Shock : 1,500 G, compliance to MIL-STD-810F
- Working well in critical environment
- Very high performance, very low power consumption
- Low weight, Noiseless

1.3. Flash Management Technology - Static Wear Leveling

In order to gain the best management for flash memory, APRO MLC micro SATA II Flash (MSF) Module – HERMES-D Series supports static wear -leveling technology to manage the Flash system. The life of flash memory is limited; the management is to increase the life of the flash product.

A static wear-leveling algorithm evenly distributes data over an entire Flash cell array and searches for the least used physical blocks. The identified low cycled sectors are used to write the data to those locations. If blocks are empty, the write occurs normally. If blocks contain static data, it moves that data to a more heavily used location before it moves the newly written data. The static wear leveling maximizes effective endurance Flash array compared to no wear leveling or dynamic wear leveling.

1.4. ECC Technology

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements an algorithm that can correct 16 bits per 512 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

1.5. Bad Block Management

Bad blocks of NAND flash may accumulate up to 2% of entire number of blocks during its manufacturing process and during the flash operational usage.
A system must be able to recognize bad block(s) based on the original bad block information and create a bad block table to keep track of blocks that fail during use. The first block of NAND Flash (block 0) is guaranteed to be good. The bad block information is stored in the reservoir area that is located in the highest address region of the NAND flash. Once the bad blocks have been located, and the bad blocks be no longer accessed.
To locate the bad blocks on a brand new device, read out each block. Any block that is not all FFFFh in 1st sector of 1st or 2nd page in a spare area is a bad block. Although random bit errors may occur during use, this does not necessarily mean that a block is bad. Generally, a block should be marked as bad only when there is a problem or erase failure. This can be determined by doing a status read after erase/program operation. The flash memory is initialized by formatting the flash memory into a reserved area and user area.

In order to detect the initial bad blocks to handle run time bad blocks, APRO HERMES-D Series' SSD provides the Bad Block Management scheme. It remaps a bad block to one of the reserved blocks so that the data contained in one bad block is not lost and new data writes on a bad block is avoided.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 1: Environmental Specification

APRO MLC micro SATA II Flash (MSF) Module HERMES-D Series		Commercial Grade
		SPMSFxxxx-JDCMM
Temperature	**Operating:**	0ºC ~ +70ºC
	Non-operating:	-20ºC ~ +80ºC
Humidity	**Operating & Non-operating:**	10% ~ 95% non-condensing
Vibration	**Operating & Non-operating:**	15G, compliance to MIL-STD-810F
Shock	**Operating & Non-operating:**	1,500G, compliance to MIL-STD-810F
Altitude	**Operating & Non-operating:**	70,000 feet

2.2. System Power Requirements

Table 2: Power Requirement

APRO MLC micro SATA II Flash (MSF) Module HERMES-D Series		Standard Grade
		SxMSFxxxx-JDCMM
DC Input Voltage (VCC)		**5V ± 5%**
3.3V Current (Maximum average value)	**Reading Mode :**	212 mA (max.)
	Writing Mode :	254 mA (max.)
	Idle Mode :	128 mA (max.)

Table 3: Power Connector

Pin No.	Connector	
Pin 1	Vcc 5V	
Pin 2	GND	

2.3. System Performance

Table 4: System Performances

Data Transfer Mode supporting		Serial ATA Gen-II (3.0Gb/s = 380MB/s)					
Random Access Time		0.1 ms					
Maximum Performance	Capacity	4GB	8GB	16GB	32GB	64GB	128GB
	Sequential Read	34	60	105	112	114	124
	Sequential Write	18	23	29	42	45	73
The number of Flash IC		1 pcs	2 pcs	4 pcs	4 pcs	4 pcs	4 pcs

Note:

(1). All values quoted are typically at 25℃ and nominal supply voltage.

(2). Testing of the APRO micro SATA II Flash Module maximum performance was performed under the following platform:

- Computer with AMD 3.0GHz processor

- Windows XP Professional operating system

2.4. System Reliability

Table 5: System Reliability

MTBF	>4,000,000 hours
Wear-leveling Algorithms	Static Wear-leveling
Bad Blocks Management	Supportive
ECC Technology	16 bits per 512 bytes in an ECC block

2.5. Physical Specifications

Refer to Table 6 and see Figure 2 for APRO MLC APRO MLC micro SATA II Flash (MSF) Module HERMES-D Series physical dimensions

Table 6: Physical Specifications

Form-factor	Width	Length:	Height:	Weight:
Vertical Type – Standard (VS)	25.85 mm	39.40 mm	8.0 mm (Housing thickness)	20.00g

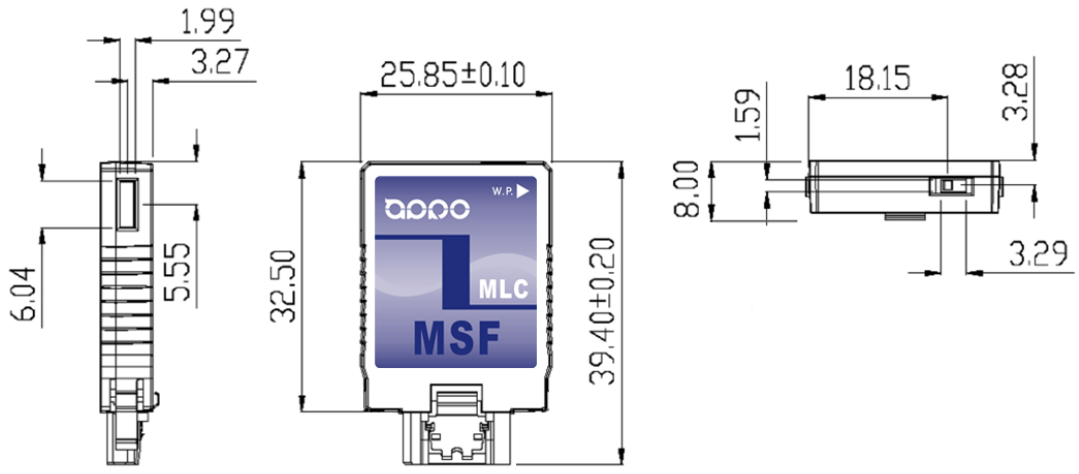

Figure 2: Dimension of micro SATA II Flash Module

2.6. Capacity Specifications

The table 7 shows the specific capacity for the various models and the default number of heads, sectors/track and cylinders.

Table 7: Device Parameters

Unformatted Capacity	Cylinder	Head	Sector	LBA
4GB	7,785	16	63	7,847,280
8GB	16,383	16	63	15,649,200
16GB	16,383	16	63	31,277,232
32GB	16,383	16	63	62,533,296
64GB	16,383	16	63	125,045,424
128GB	16,383	16	63	249,434,880

2.7. Physical Description

APRO MLC micro SATA II Flash Modules – HERMES-D Series follow standard SATA 1.0a with 7-pin signal segment. The interface is 7-pin female connector. There are 2 solutions for customer's requirement. If customer's motherboard design in the SATA interface pin-7 with 5V power output, there is one solution which is built-in power pin as the 7th pin of 7 pins header (w/fuse) , or one solution w/o fuse and for connection via cable, the cable should be no longer than 1meter.

Figure 3 is the aspect of the connector of micro SATA II Flash Module.

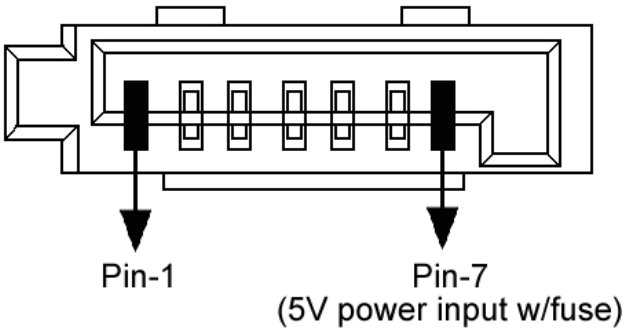

Figure 3: Front view of micro SATA II Flash Module HERMES-D Series

2.8. Pin Assignments

There are total of 7 pins in the signal segment. The pin assignments are listed in below table 8.

Table 8: Pin Assignments

Pin No.	Signal Name	Description
S1	GND	Shielding
S2	A+	Differential signal to A
S3	A-	Differential signal to A-
S4	GND	Shielding
S5	B-	Differential signal to B
S6	B+	Differential signal to B
S7	GND or VCC (+5V)	Shielding/Power

Note:

All pins are in a signal row with a 1.27 mm (0.050" pitch).

The commands on the mating sequence in forward table apply to the case of backplane blind mate connector only. In this case, the mating sequences are:

(1) The pre-charge power pins and other ground pins.

(2) The signal pins and the rest of the power pins.

3. ATA Command Register

3.1. ATA Commands

The commands supported ATA/ATAPI-7 commands; certain obsolesced commands are also supported. The supported commands are listed in Table 9.

Table 9: ATA Commands Supported

Command Name	Code	PARAMETERS USED					
		SC	SN	CY	DR	HD	FT
CHECK POWER MODE	E5h	O	X	X	O	X	X
DEVICE CONFIGURATION OVERLAY	B1h	X	X	X	O	X	O
EXECUTE DIAGNOSTICS	90h	X	X	X	O	X	X
FLUSH CACHE	E7h	X	X	X	O	X	X
FLUSH CACHE EXT	EAh	X	X	X	O	X	X
IDENTIFY DEVICE	ECh	X	X	X	O	X	X
IDLE	E3h	O	X	X	O	X	X
IDLE IMMEDIATE	E1h	X	X	X	O	X	X
NOP	00h	F	F	F	O	X	O
INITIALIZE DEVICE PARAMETERS	91h	O	X	X	O	O	X
READ BUFFER	E4h	X	X	X	O	X	X
READ DMA	C8h or C9h	O	O	O	O	O	X
READ DMA EXT	25h	O	O	O	O	O	X
READ FPDMA QUEUED	60h	O	O	O	O	O	O
READ LOG EXT	2Fh	O	O	O	O	O	O
READ MULTIPLE	C4h	O	O	O	O	O	X
READ MULTIPLE EXT	29h	O	O	O	O	O	X
READ NATIVE MAX ADDRESS	F8h	X	X	X	O	X	X
READ NATIVE MAX ADDRESS EXT	27h	X	X	X	O	X	X
READ SECTOR(S)	20h or 21h	O	O	O	O	O	X
READ SECTOR(S) EXT	24h	O	O	O	O	O	X
READ VERIFY SECTOR(S)	40h or 41h	O	O	O	O	O	X
READ VERIFY SECTOR(S) EXT	42h	O	O	O	O	O	X
RECALIBRATE	10h	X	X	X	O	X	X
SECURITY DISABLE PASSWORD	F6h	X	X	X	O	X	X
SECURITY ERASE PREPARE	F3h	X	X	X	O	X	X
SECURITY ERASE UNIT	F4h	X	X	X	O	X	X
SECURITY FREEZE LOCK	F5h	X	X	X	O	X	X
SECURITY SET PASSWORD	F1h	X	X	X	O	X	X
SECURITY UNLOCK	F2h	X	X	X	O	X	X
SEEK	7xh	X	X	O	O	O	X
SET FEATURES	EFh	O	X	X	O	X	O
SET MAX	F9h	O	O	O	O	O	O
SET MAX ADDRESS EXT	37h	O	O	O	O	O	X
SET MULTIPLE MODE	C6h	O	X	X	O	X	X
SLEEP	E6h	X	X	X	O	X	X

SMART	B0h	X	X	O	O	X	O
STANDBY	E2h	X	X	X	O	X	X
STANDBY IMMEDIATE	E0h	X	X	X	O	X	X
WRITE BUFFER	E8h	X	X	X	O	X	X
WRITE DMA	CAh or CBh	O	O	O	O	O	X
WRITE DMA EXT	35h	O	O	O	O	O	X
WRITE DMA FUA EXT	3Dh	O	O	O	O	O	X
WRITE FPDMA QUEUED	61h	O	O	O	O	O	O
WRITE LOG EXT	3Fh	O	O	O	O	O	X
WRITE MULTIPLE	C5h	O	O	O	O	O	X
WRITE MULTIPLE EXT	39h	O	O	O	O	O	X
WRITE MULTIPLE FUA EXT	CEh	O	O	O	O	O	X
WRITE SECTOR(S)	30h or 31h	O	O	O	O	O	X
WRITE SECTOR(S) EXT	34h	O	O	O	O	O	X
WRITE VERIFY	3Ch	O	O	O	O	O	O

Note:
O = Valid, X = Don't care
SC = Sector Count Register
SN = Sector Number Register
CY = Cylinder Low/High Register
DR = DEVICE SELECT Bit (DEVICE/HEAD Register Bit 4)
HD = HEAD SELECT Bit (DEVICE/HEAD Register Bit 3-0)
FT = Features Register

3.2. ATA Command Specification

3.2.1. Check Power Mode (E5h)

Features	- This command is mandatory for devices. -This command is mandatory when the Power Management feature set is implemented.
Protocol	Non-data command

Check power mode command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	Obs	DEV	Na	Na	Na	Na
Command	E5h							

Device register:

DEV *shall specify the selected device.*

4. *Identify Device (ECh)*

Features	-Mandatory for all devices. -Devices implementing the PACKET Command feature set
Protocol	PIO data-in

Identify device command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	Obs	DEV	Na	Na	Na	Na
Command	ECh							

Device register:

DEV *shall specify the selected device.*

Identify device command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description - *The IDENTIFY DEVICE command enables the host to receive parameter information from the device. When the command is issued, the device sets the BSY bit to one, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit to one, clears the BSY bit to zero, and asserts INTRQ if nIEN is cleared to zero. The host may then transfer the data by reading the Data register. In Table of Check power mode command for inputs information, which defines the arrangement and meaning of the parameter words in the buffer. All reserved bits or words shall be zero. Some parameters are defined as a 16-bit value. A word that is defined as a 16-bit value places the most significant bit of the value on signal line DD15 and the least significant bit on signal line DD0.*

Some parameters are defined as 32-bit values (e.g. words (61:60)). Such fields are transfer using two successive word transfers. The device will first transfer the least significant bits, bits (15:0) of the value, on signal lines DD(15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits(31:16) of the value, shall be transferred on DD(15:0) respectively. Some parameters are defined as a string of ASCII characters.

Device register :

DEV *shall indicate the selected device.*

Status register:

BSY *shall be cleared to zero indicating command completion.*

DRDY *shall be set to one.*

DF *(Device Fault) shall be cleared to zero.*

DRQ *shall be cleared to zero.*

ERR *shall be cleared to zero.*

4.1. Identify Device Information Default Value

Table 10: Identify Device command parameters

Word	Value	F/V	Description
0	0040h		General configuration
		F	15 0 = ATA device
		X	14-8 Retired
		X	7-6 Obsolete
		X	5-3 Retired
		V	2 Response incomplete
		X	1 Retired
			0 Reserved
1	XXXXh	F	Number of logical cylinders
2	C837h	V	Specific configuration
3	0010h	F	Number of logical heads
4-5	0000h	X	Retired
6	003Fh	F	Number of logical sector per logical track
7-8	0000h		Reserved for assignment by the CompactFlash_ Association
9	0000h	X	Retired
10-19	XXXXh	F	Serial number (20 ASCII characters)
20-21	0000h	X	Retired
22	0000h	X	Obsolete
23-26	XXXXh	F	Firmware revision (8 ASCII characters)
27-46	XXXXh	F	Model number (40 ASCII characters)
47	8010h	F	15-8 80h
		F	7-0 00h = Reserved
			01h = Maximum number of 1 sectors on READ/WRITE MULTIPLE commands
48	0000h		Reserved
49	2F00h		Capabilities
			15-14 Reserved for the IDENTIFY PACKET DEVICE command.
		F	13 1 = Standby timer values as specified in this standard are supported
			0 = Standby timer values shall be managed by the device
			12 Reserved for the IDENTIFY PACKET DEVICE command.
		F	11 1 = IORDY supported
			0 = IORDY may be supported
		F	10 1 = IORDY may be disabled
		F	9 1 = LBA supported
		F	8 1 = DMA supported.
		X	7-0 Retired
50	4000h		Capabilities
		F	15 Shall be cleared to zero.
		F	14 Shall be set to one.
			13-2 Reserved.
		X	1 Obsolete
		F	0 Shall be set to one to indicate a device specific Standby timer value minimum.
51	0000h	F	15-8 PIO data transfer cycle timing mode
			7-0 Reserved
52	0000h	X	Obsolete
53	0007h	F	15-3 Reserved

Word	Value	F/V	Description
		F	2 1 = the fields reported in word 88 are valid
			0 = the fields reported in word 88 are not valid
		F	1 1 = the fields reported in words 70:64 are valid
			0 = the fields reported in words 70:64 are not valid
		X	0 1 = the fields reported in words 58:54 are valid
			0 = the fields reported in words 58:54 are not valid
54	XXXXh	X	Number of current cylinders
55	0010h	X	Number of current heads
56	003Fh	X	Number of current sector per track
57-58	XXXXh	X	Current capacity in sectors
59	0110h		15-9 Reserved
		V	8 1 = Multiple sector setting is valid
		V	7-0 xxh = Setting for number of sectors that shall be transferred per interrupt on R/W Multiple command
60-61	XXXXh	F	Total number of user addressable sectors
62	0000h	X	Obsolete
63	0X07h		15-11 Reserved
		V	10 1 = Multiword DMA mode 2 is selected
			0 = Multiword DMA mode 2 is not selected
		V	9 1 = Multiword DMA mode 1 is selected
			0 = Multiword DMA mode 1 is not selected
		V	8 1 = Multiword DMA mode 0 is selected
			0 = Multiword DMA mode 0 is not selected
			7-3 Reserved
		F	2 1 = Multiword DMA mode 2 and below are supported
		F	1 1 = Multiword DMA mode 1 and below are supported
		F	0 1 = Multiword DMA mode 0 is supported
64	0003h		15-8 Reserved
		F	7-0 Advanced PIO modes supported
65	0078h	F	Minimum Multiword DMA transfer cycle time per word
66	0078h	F	Manufacturer's recommended Multiword DMA transfer cycle time
67	0078h	F	Minimum PIO transfer cycle time without flow control
68	0078h	F	Minimum PIO transfer cycle time with IORDY flow control
69-70	0000h		Reserved
71-74	0000h		Reserved for the IDENTIFY PACKET DEVICE command
75	001Fh		Queue depth
			15-5 Reserved
		F	4-0 Maximum queue depth - 1
76	0106h		Serial ATA Capabilities
			15-11 Reserved for Serial ATA
		F	10 1 = Supports Phy Event Counts
		F	9 1 = Supports receipt of host initiated power management requests
		F	8 1 = Supports the NCQ feature set
			7-3 Reserved for Serial ATA
		F	2 1 = Supports SATA Gen2 Signaling Speed (3.0Gb/s)
		F	1 1 = Supports SATA Gen1 Signaling Speed (1.5Gb/s)
		F	0 Shall be cleared to zero
77	0000h		Reserved for Serial ATA
78	0044h		Serial ATA feature supported
			15-7 Reserved for Serial ATA

Word	Value	F/V	Description
		F	6 1 = Device supports Software Settings Preservation
			5 Reserved for Serial ATA
		F	4 1 = Device supports in-order data delivery
		F	3 1 = Device supports initiating power management
		F	2 1 = Device supports DMA Setup auto-activation
		F	1 1 = Device supports non-zero buffer offsets
		F	0 Shall be cleared to zero
79	0040h		Serial ATA feature enabled
			15-7 Reserved for Serial ATA
		V	6 1 = Software Settings Preservation enabled
			5 Reserved for Serial ATA
		V	4 1 = In-order data delivery enabled
		V	3 1 = Device initiated power management enabled
		V	2 1 = DMA Setup auto-activation enabled
		V	1 1 = Non-zero buffer offsets enabled
		F	0 Shall be cleared to zero
80	01F0h		Major version number 0000h or FFFFh = device does not report version
			15 Reserved
		F	14 Reserved for ATA/ATAPI-14
		F	13 Reserved for ATA/ATAPI-13
		F	12 Reserved for ATA/ATAPI-12
		F	11 Reserved for ATA/ATAPI-11
		F	10 Reserved for ATA/ATAPI-10
		F	9 Reserved for ATA/ATAPI-9
		F	8 Reserved for ATA/ATAPI-8
		F	7 1 = supports ATA/ATAPI-7
		F	6 1 = supports ATA/ATAPI-6
		F	5 1 = supports ATA/ATAPI-5
		F	4 1 = supports ATA/ATAPI-4
		F	3 Obsolete
		X	2 Obsolete
		X	1 Obsolete
			0 Reserved
81	0000h	F	Minor version number
82	746Bh		Command and feature sets supported
		X	15 Obsolete
		F	14 1 = NOP command supported
		F	13 1 = READ BUFFER command supported
		F	12 1 = WRITE BUFFER command supported
		X	11 Obsolete
		F	10 1 = Host Protected Area feature set supported
		F	9 1 = DEVICE RESET command supported
		F	8 1 = SERVICE interrupt supported
		F	7 1 = release interrupt supported
		F	6 1 = look-ahead supported
		F	5 1 = write cache supported
		F	4 Shall be cleared to zero to indicate that the PACKET Command feature set is not
		F	supported.
		F	3 1 = mandatory Power Management feature set supported
		F	2 1 = Removable Media feature set supported
		F	1 1 = Security Mode feature set supported
			0 1 = SMART feature set supported
83	7D08h		Command and feature sets supported
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13 1 = The FLUSH CACHE EXT command is supported
		F	12 Shall be set to one to indicate that the mandatory FLUSH CACHE command is

Word	Value	F/V	Description	
		F	supported	
		F	11	1 = The DCO feature set is supported
		F	10	1 = The 48-bit Address feature set is suported
		F	9	1 = The AAM feature set is supported
			8	1 = SET MAX security extension supported
		F	7	Reserved
		F	6	1 = SET FEATURES subcommand required to spinup after power-up
		F	5	1 = Power-Up In Standby feature set supported
		F	4	1 = Removable Media Status Notification feature set supported
		F	3	1 = Advanced Power Management feature set supported
		F	2	1 = CFA feature set supported
		F	1	1 = READ/WRITE DMA QUEUED supported
			0	1 = DOWNLOAD MICROCODE command supported
84	4040h	F	15	Shall be cleared to zero
		F	14	Shall be set to one
		F	13	1 = The IDLE IMMEDIATE command with UNLOAD feature is supported
			12-11	Reserved for TLC
		X	10-9	Obsolete
		F	8	1 = The 64-bit World wide name is supported
		F	7	1 = The WRITE DMA QUEUED FUA EXT command is supported
		F	6	1 = The WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are
		F	supported	
		F	5	1 = The GPL feature set is supported
		F	4	1 = The Streaming feature set is supported
		F	3	1 = The Media Card Pass Through Command feature set is supported
		F	2	1 = Media serial number is supported
		F	1	1 = SMART self-test supported
			0	1 = SMART error logging supported
85	746Xh		Command and feature sets supported or enable	
		X	15	Obsolete
		F	14	1 = The NOP command is supported
		F	13	1 = The READ BUFFER command is supported
		F	12	1 = The WRITE BUFFER command is supported
		X	11	Obsolete
		V	10	1 = HPA feature set is supported
		F	9	Shall be cleared to zero to indicate that the DEVICE RESET command is not
		V	supported	
		V	8	1 = The SERVICE interrupt is enabled
		V	7	1 = The release interrupt is enabled
		V	6	1 = Read look-ahead is enabled
		F	5	1 = The volatile write cache is enabled
		F	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not
		X	supported.	
		V	3	Shall be set to one to indicate that the mandatory Power Management feature is
		V	supported	
			2	Obsolete
			1	1 = The Security feature set is enabled
			0	1 = The SMART feature set is enabled
86	BC00h		Command and feature sets supported or enable	
		F	15	1 = Words 119-120 are valid
			14	Reserved
		F	13	1 = FLUSH CACHE EXT command supported
		F	12	1 = FLUSH CACHE command supported
		F	11	1 = The DCO feature set is supported
		F	10	1 = The 48-bit Address feature set is supported
		V	9	1 = The AAM feature set is enable
		V	8	1 = The SET MAX security extension is enabled by SET MAX SET PASSWORD
			7	Reserved for Address Offset Reserved Area Boot Method

Word	Value	F/V	Description
		F	6 1 = SET FEATURES subcommand required to spin-up after power-up
		V	5 1 = The PUIS feature set is enabled
		X	4 Obsolete
		V	3 1 = The APM feature set is enabled
		F	2 1 = The CFA feature set is supported
		F	1 1 = The TCQ feature set is supported
		F	0 1 = The DOWNLOAD MICROCODE command is supported
87	4040h		Command and feature sets supported or enabled
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13 1 = The IDLE IMMEDIATE command with UNLOAD feature is supported
			12-11 Reserved for TLC
		X	10-9 Obsolete
		F	8 1 = The 64-bit World wide name is supported
		F	7 1 = The WRITE DMA QUEUED FUA EXT command is supported
		F	6 1 = The WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are
		F	supported
		X	5 1 = The GPL feature set is supported
		V	4 Obsolete
		V	3 1 = The Media Card Pass Through Command feature set is supported
		F	2 1 = Media serial number is supported
		F	1 1 = SMART self-test supported
			0 1 = SMART error logging supported
88	XX7Fh		Ultra DMA modes
			15 Reserved
		V	14 1 = Ultra DMA mode 6 is selected
			0 = Ultra DMA mode 6 is not selected
		V	13 1 = Ultra DMA mode 5 is selected
			0 = Ultra DMA mode 5 is not selected
		V	12 1 = Ultra DMA mode 4 is selected
			0 = Ultra DMA mode 4 is not selected
		V	11 1 = Ultra DMA mode 3 is selected
			0 = Ultra DMA mode 3 is not selected
		V	10 1 = Ultra DMA mode 2 is selected
			0 = Ultra DMA mode 2 is not selected
		V	9 1 = Ultra DMA mode 1 is selected
			0 = Ultra DMA mode 1 is not selected
		V	8 1 = Ultra DMA mode 0 is selected
			0 = Ultra DMA mode 0 is not selected
			7 Reserved
		F	6 1 = Ultra DMA mode 6 and below are supported
		F	5 1 = Ultra DMA mode 5 and below are supported
		F	4 1 = Ultra DMA mode 4 and below are supported
		F	3 1 = Ultra DMA mode 3 and below are supported
		F	2 1 = Ultra DMA mode 2 and below are supported
		F	1 1 = Ultra DMA mode 1 and below are supported
		F	0 1 = Ultra DMA mode 0 is supported
89	001Eh		15-8 Reserved
		F	7-0 Time required for Normal Erase mode SECURITY ERASE UNIT command
90	001Eh		15-8 Reserved
		F	7-0 Time required for Enhanced Erase mode SECURITY ERASE UNIT command
91	0000h	V	Current APM level value
92	FFFEh	V	Master Password Identifier
93	0000h	X	Hardware reset result
94	0000h		Current AAM value
		F	15-8 Vendor's recommended AAM value

Word	Value	F/V	Description
		V	7-0 Current AAM value
95-99	0000h		Reserved
100-103	XXXXh	X	Total Number of User Addressable Logical Sectors for 48-bit commands (QWord)
104-105	0000h		Reserved
106	4000h		Physical sector size / logical sector size
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13 1 = Device has multiple logical sectors per physical sector
		F	12 1 = Device Logical Sector longer than 256 Words
			11-4 Reserved
		F	3-0 2x logical sectors per physical sector
107	0000h	F	Inter-seek delay for ISO 7779 standard acoustic testig
108-111	XXXXh	F	Worldwide name
112-115	0000h		Reserved
116	0000h		Reserved for TLC
117-118	0000h	F	Logical sector size (DWord)
119	4000h		Commands and feature sets supported (Continued from words 84:82)
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
			13-6 Reserved
		F	5 1= The Free-fall Control feature set is supported
		F	4 1 = The DOWNLOAD MICROCODE command with mode 3 is supported
		F	3 1 = The READ LOG DMA EXT and WRITE LOG DMA EXT commands are
		F	supported
		F	2 1 = The WRITE UNCORRECTABLE EXT command is supported
			1 1 = The Write-Read-Verify feature set is supported
			0 Reserved for DDT
120	4000h		Commands and feature sets supported or enabled (Continued from words 87:85)
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
			13-6 Reserved
		V	5 1= The Free-fall Control feature set is enabled
		F	4 1 = The DOWNLOAD MICROCODE command with mode 3 is supported
		F	3 1 = The READ LOG DMA EXT and WRITE LOG DMA EXT commands are
		F	supported
		V	2 1 = The WRITE UNCORRECTABLE EXT command is supported
			1 1 = The Write-Read-Verify feature set is enabled
			0 Reserved for DDT
121-126	0000h		Reserved for expended supported and enabled settings
127	0000h	X	Obsolete
128	0021h		Security status
			15-9 Reserved
		V	8 Security level 0 = High, 1 = Maximum
			7-6 Reserved
		F	5 1 = Enhanced security erase supported
		V	4 1 = Security count expired
		V	3 1 = Security frozen
		V	2 1 = Security locked
		V	1 1 = Security enabled
		F	0 1 = Security supported
129-159	0000h	X	Vendor specific

Word	Value	F/V	Description
160	0000h		CFA power mode
		F	15 Word 160 supported
			14 Reserved
		F	13 CFA power mode 1 is required for one or more commands implemented by the
		V	device
		F	12 CFA power mode 1 disabled
			11:0 Maximum current in ma
161-167	0000h		Reserved for the Compact Flash Association
168	0003h		15:4 Reserved
		F	3:0 Device Nominal Form Factor
169	0000h		DATA SET MANAGEMENT is supported
			15:1 Reserved
		F	0 1 = the Trim bit in the DATA SET MANAGEMENT is supported
170-173	0000h	F	Additional Product Identifier (ATA String)
174-175	0000h		Reserved
176-205	0000h	V	Current media serial number (ATA String)
206	0000h		SCT Command Transport
		X	15:12 Vendor Specific
			11:6 Reserved
		F	5 The SCT Data Tables command is supported
		F	4 The SCT Feature Control command is supported
		F	3 The SCT Error Recovery Control command is supported
		F	2 The SCT Write Same command is supported
		F	1 Obsolete
		F	0 The SCT Command Transport is supported
207-208	0000h		Reserved for CE-ATA
209	4000h		Alignment of logical blocks within a physical block
			15 Shall be cleared to zero
			14 Shall be set to one
		F	13:0 Logical sector offset within the first physical sector where the first logical sector is
			placed
210-211	0000h	V	Write-Read-Verify Sector Count Mode 3 (DWord)
212-213	0000h	F	Write-Read-Verify Sector Count Mode 2 (DWord)
214	0000h		NV Cache Capabilities
		F	15:12 NC+V Cache feature set version
		F	11:8 NV Cache Power Mode feature set version
			7:5 Reserved
		V	4 1 = NV Cache feature set enabled
			3:2 Reserved
		V	1 1 = NV Cache Power Mode feature set enabled
		F	0 1 = NV Cache Power Mode feature set supported
215-216	0000h	V	NV Cache Size in Logical Blocks (DWord)
217	0001h	F	Nominal media rotation rate
218	0000h		Reserved
219	0000h	F	NV Cache Options
			15:8 Reserved
			7:0 Device Estimated Time to Spin Up in Seconds
220	0000h	V	15:8 Reserved
			7:0 Write-Read-Verify feature set current mode
221	0000h		Reserved
222	101Fh		Transport major version number

Word	Value	F/V	Description
			0000h or FFFFh = device does not report version
		F	15:12 Transport Type 0h = Parallel 1h = Serial 2h-Fh = Reserved
			Parallel Serial
			11:5 Reserved Reserved
		F	4 Reserved SATA Rev 2.6
		F	3 Reserved SATA Rev 2.5
		F	2 Reserved SATA II: Extensions
		F	1 ATA/ATAPI-7SATA 1.0a
		F	0 ATA8-APT ATA8-AST
223	0000h	F	Transport minor version number
224-233	0000h		Reserved for CE-ATA
234	0000h	F	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 3
235	0000h	F	Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 3
236-254	0000h		Reserved
255	XXXXh		Integrity word
		V	15-8 Checksum
		V	7-0 Checksum Validity Indicator

Key:
F/V – Fixed/variable content
F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.
V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device.
X = the content of the word may be fixed or variable.

4.1.1. IDLE (E3h)

Features	Power Management Feature Set
Protocol	Non-Data

Values other than zero in the Sector Count register when the IDLE command is issued shall determine the time period programmed into the Standby timer.

Idle command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Timer period value							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	Obs	DEV	Na	Na	Na	Na
Command	E3h							

Device register :

DEV *shall specify the selected device.*

Idle command sector count register contents information

Sector Count register contents	Corresponding timeout period
0 (00h)	Timeout disabled
1-240 (01h-F0h)	(value*5)s
241-251 (F1h-FBh)	((Value-240)*30)min
252 (FCh)	21min
253 (FDh)	Period between 8 and 12 hrs
254 (FEh)	Reserved
255 (FFh)	21 min 15 s
NOTE – Times are approximate	

Idle command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register -

DEV *shall indicate the selected device.*

Status register -

BSY *will be cleared to zero indicating command completion.*

DRDY *will be set to one.*

DF *(Device Fault) will be cleared to zero.*

DRQ *shall be cleared to zero.*

ERR *shall be cleared to zero.*

Idle command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *The IDLE command allows the host to place the device in the idle mode and also set the Standby timer.*

Status register:

DRDY set to one

4.1.2. Idle Immediate (E1h)

Features	Power Management Feature Set
Protocol	Non-Data

Idle immediate command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Command	E1h							

Device register:
DEV *shall specify the selected device.*

Idle immediate command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *The IDLE IMMEDIATE command allows the host to immediately place the device in the idle mode.*
Device Register:
DEV *shall indicate the selected device.*
Status register:
BSY *will be cleared to zero indicating command completion.*
DRDY *will be set to one.*
DF *(Device Fault) will be cleared to zero.*
DRQ *shall be cleared to zero.*
ERR *shall be cleared to zero.*

4.1.3. S.M.A.R.T. Function (Self-Monitoring, Analysis, and Reporting Technology)

To perform different processing requires predicting device failures, according to the subcommand specified in the Features register.

SMART Feature registers values

Value	Command
D0h	SMATR Read Data
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS

4.1.4. S.M.A.R.T. Read Data (D0h)

Features	Operation when the SMART feature set is implemented.
Protocol	PIO data-in

SMART command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register:

DEV *shall specify the selected device.*

SMART command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:

DEV *shall indicate the selected device.*

Status registers:

BSY *will be cleared to zero indicating command completion.*

DRDY *will be set to one. SMART enabled.*

DF *(Device Fault) will be cleared to zero.*

DRQ *shall be cleared to zero.*

ERR *shall be cleared to zero*.

ID of SMART data structure

	+0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+10	+11
Attribute Name	ID	Flags		Init	Worst	Raw Attribute Value						Rsv
Read Error Rate	01h	0Bh	00h	64h	64h	FFh	FFh	FFh	00h	00h	00h	00h
Throughput Performance	02h	05h	00h	64h	64h	00h	00h	00h	00h	00h	00h	00h
Spin Up Time	03h	07h	00h	64h	64h	00h	00h	00h	00h	00h	00h	00h
Reallocated Sector Count	05h	13h	00h	64h	64h	00h	00h	00h	00h	00h	00h	00h
Seek Error Rate	07h	0Bh	00h	64h	64h	00h	00h	00h	00h	00h	00h	00h
Seek Time performance	08h	05h	00h	64h	64h	00h	00h	00h	00h	00h	00h	00h
Power-On hours Count	09h	12h	00h	64h	64h	(1)		00h	00h	00h	00h	00h
Spin Retry Count	0Ah	13h	00h	64h	64h	00h	00h	00h	00h	00h	00h	00h
Drive Power Cycle Count	0Ch	12h	00h	64h	64h	(2)		00h	00h	00h	00h	00h
SATA PHY Error Count	A8h	12h	00h	64h	64h	(3)		00h	00h	00h	00h	00h
Bad Block Count	AAh	03h	00h	64h	64h	00h	00h	(4)		(5)		00h
Erase Count	ADh	12h	00h	64h	64h	(6)		(7)		(6)	(7)	00h
Bad Cluster Table Count	AFh	03h	00h	64h	64h	(8)		00h	00h	00h	00h	00h
Unexpected Power Loss Count	C0h	12h	00h	64h	64h	(9)		00h	00h	00h	00h	00h
Temperature	C2h	22h	00h	(10)	64h	(10)	00h	(11)	00h	(12)	00h	00h
Current Pending Sector Counter	C5h	12h	00h	64h	64h	00h	00h	00h	00h	00h	00h	00h
Write Head	F0h	13h	00h	64h	64h	00h	00h	00h	00h	00h	00h	00h

Smart command for AVERAGE/MAX ERASE count information

	SMART	DI 101
	F: Fixed V:Variable X: None	
Byte	F/V	Description
0-188	X	
189-190	F	Total Bad Block Number of System(190:MSB 189:LSB)
191-192	F	Later Bad Block Number of System(192:MSB 191:LSB)
193-198	X	
199-200.203	F	Average Erase Count(203:MSB 199:LSB)
201-202.204	V	Maximum Erase Count(204:MSB 201:LSB)
205-510	X	
511	V	Check Sum

When the Maximum erase count is 255 bigger than average erase count, the wear-leveling will be executed.

4.1.5. S.M.A.R.T. ENABLE OPERATIONS (D8h)

Features	Smart Feature Set
Protocol	Non-data

SMART Enable command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register:

DEV *shall specify the selected device.*

SMART command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register:

DEV *shall indicate the selected device.*

Status register:

BSY *will be cleared to zero indicating command completion.*

DRDY *will be set to one. (This command enables access to all SMART capabilities within device.)*

DF *(Device Fault) will be cleared to zero.*

DRQ *shall be cleared to zero.*

ERR *shall be cleared to zero.*

4.1.6. SMART DISABLE OPERATIONS (D9h)

Features	Smart Feature Set
Protocol	Non-data

SMART DISABLE Command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register:

***DEV** shall specify the selected device.*

SMART command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

***Description:** This command disables all SMART capabilities within device.*
Device Register:
***DEV** shall indicate the selected device.*
Status register:
***BSY** will be cleared to zero indicating command completion.*
***DRDY** will be set to one. SMART enabled.*
***DF** (Device Fault) will be cleared to zero.*
***DRQ** shall be cleared to zero.*
***ERR** shall be cleared to zero.*

4.1.7. Read Multiple (C4h)

Protocol	PIO data-in

Read multiple command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C4h							

Sector Count:
Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.
LBA Low:
Starting LBA bits (7:0).
LBA Mid:
Starting LBA bits (15:8)
LBA High:
Starting LBA bits (23:16)
Device:
***DEV** shall specify the selected device.*
Bit (3:0) starting LBA bits (27:24)

Read multiple command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:
DEV *shall specify the selected device.*
Status register:
BSY *will be cleared to zero indicating command completion*
DRDY *will be set to one.*
DF *(Device Fault) will be cleared to zero.*
DRQ *will be cleared to zero*
ERR *will be cleared to zero.*

Read multiple command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *This command reads the number of sectors specified in the sector Count register. The number of sectors per block is defined by the content of word 59 in the IDENTIFY DEVICE response.*
An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred us indeterminate.
Error register:
UNC *shall be set to one if data is uncorrectable.*
IDNF *shall be set to one if a user-accessible address is requested could not be found.*
LBA Low, LBA Mid, and LBA High, Device
Shall be written with the address of first unrecoverable error.
Status register:
BSY *will be cleared to zero indicating command completion*
DRDY *will be set to one.*
DF *(Device Fault) will be cleared to zero.*
DRQ *will be cleared to zero*
ERR *will be set to one if an Error register bit is set to one.*

4.1.8. Read Sector(s) (20h)

Protocol	PIO data-in

Read sector command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	20h							

Sector Count:

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low:

Starting LBA bits (7:0).

LBA Mid:

Starting LBA bits (15:8)

LBA High:

Starting LBA bits (23:16)

Device:

DEV *shall specify the selected device.*

Bit (3:0) starting LBA bits (27:24)

Read sector command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:

DEV *shall specify the selected device.*

Status register:

BSY *will be cleared to zero indicating command completion*

DRDY *will be set to one.*

DF *(Device Fault) will be cleared to zero.*

DRQ *will be cleared to zero*

ERR *will be cleared to zero.*

Read sector command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. This transfer shall begin at the sector specified in the LBA Low, LBA Mid, LBA High, and Device registers.*

The DRQ bit is always set to one prior to data transfer regardless of the presence or absence of an error condition. The device shall interrupt for each DRQ block transferred.

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred us indeterminate.

Error register:

UNC *shall be set to one if data is uncorrectable.*

IDNF *shall be set to one if a user-accessible address is requested could not be found.*

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register:

BSY *will be cleared to zero indicating command completion*

DRDY *will be set to one.*

DF *(Device Fault) will be cleared to zero.*

DRQ *will be cleared to zero*

ERR *will be set to one if an Error register bit is set to one.*

4.1.9. Read Verify Sector (40h)

Protocol	Non-data

Read verify sector command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	40h							

Sector Count:

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low:

Starting LBA bits (7:0).
LBA Mid:
Starting LBA bits (15:8)
LBA High:
Starting LBA bits (23:16)
Device:
The LBA bit shall be set to one to specify the address is an LBA.
DEV *shall specify the selected device.*
Bit (3:0) starting LBA bits (27:24)

Read verify sector command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:

DEV *shall specify the selected device.*

Status register:

BSY *will be cleared to zero indicating command completion*
DRDY *will be set to one.*
DF *(Device Fault) will be cleared to zero.*
DRQ *will be cleared to zero*
ERR *will be cleared to zero.*

Read verify sector command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *This command is identical to the READ SECTOR(s) command, except that the device shall have read the data from the SSD, the DRQ bit is never set to one, and no data is transferred to the host.*
An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred.
Error register:
UNC *shall be set to one if data is uncorrectable.*
IDNF *shall be set to one if a user-accessible address could not be found.*
LBA Low, LBA Mid, and LBA High, Device
Shall be written with the address of first unrecoverable error.
Status register:
BSY *will be cleared to zero indicating command completion*

***DRDY** will be set to one.*
***DF** (Device Fault) will be cleared to zero.*
***DRQ** will be cleared to zero*
***ERR** will be set to one if an Error register bit is set to one.*

4.1.10. Read DMA (C8h)

Protocol	DMA

Read DMA command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C4h							

Sector Count:
Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.
LBA Low:
Starting LBA bits (7:0).
LBA Mid:
Starting LBA bits (15:8)
LBA High:
Starting LBA bits (23:16)
Device:
***DEV** shall specify the selected device.*
Bit (3:0) starting LBA bits (27:24)

Read DMA command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:
***DEV** shall specify the selected device.*
Status register:
***BSY** will be cleared to zero indicating command completion*
***DRDY** will be set to one.*
***DF** (Device Fault) will be cleared to zero.*
***DRQ** will be cleared to zero*

***ERR** will be cleared to zero.*

Read DMA command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	ICRC	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

***Description:** The READ DMA command allows the host to read data using the DMA data transfer protocol. An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred us indeterminate.*

Error register:

***ICRC** shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.*

***UNC** shall be set to one if data is uncorrectable.*

***IDNF** shall be set to one if a user-accessible address could not be found.*

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register:

***BSY** will be cleared to zero indicating command completion*

***DRDY** will be set to one. The host shall initialize the DMA channel.*

***DF** (Device Fault) will be cleared to zero.*

***DRQ** will be cleared to zero*

***ERR** will be set to one if an Error register bit is set to one.*

4.1.11. Set Multiple Mode (C6h)

Protocol	Non-data

Set multiple mode command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector per block							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	C6h							

***Description:** If the content of the Sector Count Register is not zero, then the Sector Count register contains the number of sectors per block for the device to be used on all following READ/WRITE MULTIPLE commands. The content of the Sector Count register shall be less than or equal to the value*

in bits (7:0) in word 47 in the IDENTIFY DEVICE information. The host should set the content of the Sector Count register to 1.

Set multiple mode command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:
DEV *shall specify the selected device.*
Status register
BSY *will be cleared to zero indicating command completion*
DRDY *will be set to one.*
DF *(Device Fault) will be cleared to zero.*
DRQ *will be cleared to zero*
ERR *will be cleared to zero.*

Set multiple mode command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	obs	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *This command establishes the block count for READ MULTIPLE, READ MULTI EXT, WRITE MULTIPLE. SSD can only support 1 sector per block.*
Status register:
BSY *will be cleared to zero indicating command completion*
DRDY *will be set to one.*
DF *(Device Fault) will be cleared to one if a device fault has occurred.*
DRQ *will be cleared to zero*
ERR *will be set to one if an Error register bit is set to one.*

4.1.12. Set Sleep Mode (E6h)

Protocol	Non-data

Set sleep mode for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E6h							

Device register:

DEV shall specify the selected device.

Set sleep mode for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:

DEV shall specify the selected device.

Status register:

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Set sleep mode for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: This command is the only way to cause the device to enter Sleep mode.

Status register:

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero
ERR will be set to one if an Error register bit is set to one.

4.1.13. Flush Cache (E7h)

Protocol	Non-data

Flush cache command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E7h							

Device register:
DEV *shall specify the selected device.*

Flush cache command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:
DEV *shall specify the selected device.*
Status register:
BSY *will be cleared to zero indicating command completion*
DRDY *will be set to one.*
DF *(Device Fault) will be cleared to zero.*
DRQ *will be cleared to zero*
ERR *will be cleared to zero.*

Flush cache command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							

LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description:*This command is used by the host to request the device to flush the write cache. If there is data in write cache, that data shall be written to the SSD. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.*

Error register:

ABRT *may be set to one if the device is not able to complete the action requested by the command.*

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register:

BSY *will be cleared to zero indicating command completion*

DRDY *will be set to one.*

DF *(Device Fault) will be cleared to one if a device fault has occurred.*

DRQ *will be cleared to zero*

ER*R will be set to one if an Error register bit is set to one.*

4.1.14. Standby (E2h)

Protocol	Non-data

Standby command for INPUTS information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Features	Na							
Sector Count	Time period value							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E2h							

Description: *The value in the Sector Count register when the STANDBY command is issued shall determine the time period programmed into the Standby timer.*

Device register:

DEV *shall specify the selected device.*

Standby command for NORMAL OUTPUTS information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:
DEV *shall specify the selected device.*
Status register:
BSY *will be cleared to zero indicating command completion*
DRDY *will be set to one.*
DF *(Device Fault) will be cleared to zero.*
DRQ *will be cleared to zero*
ERR *will be cleared to zero.*

Standby command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description : *This command causes the device to enter the Standby mode. If the Sector Count register is non-zero then Standby timer shall be enabled. The value in the Sector Count register shall be used determine the time programmed into the Standby timer. If the Sector Count register is zero then the Standby timer is disabled.*
Error register:
ABRT may be set to one if the device is not able to complete the action requested by the command.
Status register:
BSY *will be cleared to zero indicating command completion*
DRDY *will be set to one.*
DF *(Device Fault) will be set to one if a device fault has occurred.*
DRQ *will be cleared to zero*
ERR *will be set to one if an Error register bit is set to one.*

4.1.15. Standby Immediate (E0h)

Protocol	Non-data

Standby immediate command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E0h							

Device register:
DEV *shall specify the selected device.*

Standby immediate command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:
DEV *shall specify the selected device.*
Status register:
BSY *will be cleared to zero indicating command completion*
DRDY *will be set to one.*
DF *(Device Fault) will be cleared to zero.*
DRQ *will be cleared to zero*
ERR *will be cleared to zero.*

Standby immediate command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description : *This command causes the device to immediately enter the Standby mode.*
Error register:
ABRT *may be set to one if the device is not able to complete the action requested by the command.*
Status register:
BSY *will be cleared to zero indicating command completion*
DRDY *will be set to one.*
DF *(Device Fault) will be set to one if a device fault has occurred.*
DRQ *will be cleared to zero*
ERR *will be set to one if an Error register bit is set to one.*

4.1.16. Write Multiple (C5h)

Protocol	PIO data-out

Write multiple command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C5h							

Description : *The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.*

Sector Count:

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low:

Starting LBA bits (7:0)

LBA Mid:

Starting LBA bits (15:8)

LBA High:

Starting LBA bits (23:16)

Device:

The LBA bit shall be set to one to specify the address is an LBA.

DEV *shall specify the selected device.*

Bits(3:0) starting LBA bits (27:24)

Write multiple command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:

DEV *shall specify the selected device.*

Status register:

BSY *will be cleared to zero indicating command completion*

DRDY *will be set to one.*

DF *(Device Fault) will be cleared to zero.*

DRQ *will be cleared to zero*

ERR *will be cleared to zero.*

Write multiple command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	WP	MC	IDNF	MCR	ABRT	NM	Na
Sector Count	Na							

LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *This command writes the number of sectors specified in the Sector Count register. The number of sectors per block is defined by the content of word 59 of the IDENTIFY DEVICE response. When the WRITE MULTIPLE command is issued, the SECTOR Count register contains the number of sectors (not the number of blocks) requested. The device shall interrupt for each DRQ block transferred. IF the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where: N = Remainder (sector count / block count).*

If the WRITE MULTIPLE command is received when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with command aborted.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The command ends with the sector in error, even if the error was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupt pending is set when the DRQ bit is set to one at the beginning of each block or partial block.

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block register contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Error register:

IDNF *shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range user-accessible address is requested if command aborted is not returned.*

ABRT *shall be set to one if an error, include an ICRC error, has occurred during an Ultra DMA data transfer.*

ABRT *shall be set to one if an address outside of the range of user-accessible address is requested if IDNF is not set to one.*

LBA Low, LBA Mid, and LBA High, Device -

Shall be written with the address of first unrecoverable error.

Status register:

BSY *will be cleared to zero indicating command completion*

DRDY *will be set to one. (If bit 8 of IDENTIFY DEVICE word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.)*

DF *(Device Fault) will be set to one if a device fault has occurred.*

DRQ *will be cleared to zero*

ERR *will be set to one if an Error register bit is set to one.*

4.1.17. Write Sector (30h)

Protocol	PIO data-out

Write sector command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							

LBA High	LBA(23:16)				
Device	obs	LBA	obs	DEV	LBA(27:24)
Command	30h				

Description: *The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.*

Sector Count:

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low:

Starting LBA bits (7:0)

LBA Mid:

Starting LBA bits (15:8)

LBA High:

Starting LBA bits (23:16)

Device:

The LBA bit shall be set to one to specify the address is an LBA.

DEV *shall specify the selected device.*

Bits(3:0) starting LBA bits (27:24)

Write sector command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:

DEV *shall specify the selected device.*

Status register:

BSY *will be cleared to zero indicating command completion*

DRDY *will be set to one.*

DF *(Device Fault) will be cleared to zero.*

DRQ *will be cleared to zero*

ERR *will be cleared to zero.*

Write sector command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	WP	MC	IDNF	MCR	ABRT	NM	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The device shall interrupt for each DRQ block transferred.*

An unrecoverable error encountered during the execution if this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Error register:

***IDNF** shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.*

ABRT shall be set to one if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register:

***BSY** will be cleared to zero indicating command completion*

***DRDY** will be set to one.*

***DF** (Device Fault) will be set to one if a device fault has occurred.*

***DRQ** will be cleared to zero*

***ERR** will be set to one if an Error register bit is set to one.*

4.1.18. Write DMA (CAh)

Protocol	DMA

Write DMA command for INPUTS information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	LBA	obs	DEV	LBA(27:24)			
Command	CAh							

***Description:** The LBA Mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.*

Sector Count:

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low:

Starting LBA bits (7:0)

LBA Mid:

Starting LBA bits (15:8)

LBA High:

Starting LBA bits (23:16)

Device:

The LBA bit shall be set to one to specify the address is an LBA.

***DEV** shall specify the selected device.*

Bits (3:0) starting LBA bits (27:24)

Write DMA command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:

DEV *shall specify the selected device.*

Status register:

BSY *will be cleared to zero indicating command completion*

DRDY *will be set to one.*

DF *(Device Fault) will be cleared to zero.*

DRQ *will be cleared to zero*

ERR *will be cleared to zero.*

Write DMA command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	ICRC	WP	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *The Write DMA command allows the host to write data using the DMA data transfer protocol.*

Error register:

ICRC *shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.*

IDNF *shall be set to one if a user-accessible address could not be found. INDF shall be set to one if an address outside of the range of user-accessible address is requested if command aborted is not returned.*

ABRT *shall be set to one if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.*

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register:

BSY *will be cleared to zero indicating command completion*

DRDY *will be set to one. (The host shall initialize the DMA channel.)*

DF *(Device Fault) will be set to one if a device fault has occurred.*

DRQ *will be cleared to zero*

ERR *will be set to one if an Error register bit is set to one.*

4.1.19. Execute Device Diagnostic (90h)

Feature	General feature set
Protocol	Device diagnostic

Execute device diagnostic command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	90h							

Description: *Only the command code (90h). All other registers shall be ignored.*
Device:
DEV *shall be ignored.*

Execute device diagnostic command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Diagnostic Code							
Sector Count	Signature							
LBA Low	Signature							
LBA Mid	Signature							
LBA High	Signature							
Device	Signature							
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *The diagnostic code written into the Error register is an 8-bit code.*
Error register:
Diagnostic Code
Sector Count, LBA Low, LBA Mid, LBA High, Device registers
Device signature
Device register:
DEV *shall be cleared to zero.*

Execute device diagnostic command for status register information

Code	Description
01h	Device passed
Others	Device failed

Execute device diagnostic command for ERROR OUTPUTS information

Description: *In Table of Identify device command for normal outputs information shows the error information that is returned as a diagnostic code in the Error register. This command shall cause the devices to perform the internal diagnostic tests. This command shall be accepted regardless of the state of DRDY.*

4.1.20. Security Set Password (F1h)

Feature	Security Mode feature set
Protocol	PIO data-out

Security set password command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F1h							

Device:

DEV *shall specify the selected device.*

Security set password command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV *shall indicate the selected device.*

Status register

BSY *will be cleared to zero indicating command completion*

DRDY *will be set to one.*

DF *(Device Fault) will be set to zero.*

DRQ *will be cleared to zero*

ERR *will be set to zero.*

Security set password command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *This command transfer 512 byte of data from the host. In Table of Identify device command for normal outputs information, it defines the content of this information. The data transferred controls the function of this command. In Table of Identify device command parameters, it defines the interaction of the identifier and security level bits.*

The revision code field shall be returned in the IDENTIFY DEVICE word 92. The valid revision codes are 0001h through FFFEh. A value of 0000h or FFFFh indicates that the Master Password Revision Code is not supported.

Error Register:

ABRT *may be set to one if the device is not able to complete the action requested by the command*

Device register:

DEV *shall indicate the selected device.*

Status register:

BSY *will be cleared to zero indicating command completion*

DRDY *will be set to one.*

DF *(Device Fault) should be set to one if a device fault has occurred.*

DRQ *will be cleared to zero*

ERR *will be set to one if an Error register bit is set to one.*

Security set password command's data content

Word	Content
0	Control Word Bit 0 Identifier 0=set User password 1=set Master password Bits (7:1) Reserved Bit(8) Security level 0=High 1=Maximum Bits(15:9) Reserved
1-16	Password(32 bytes)
17	Master Password Revision Code()
18-255	Reserved

Security Set password command's identifier and security level bit interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the

		new User password. The Lock mode shall be enabled from the next power-on or hardware reset. The device shall than be unlocked by either the User password it the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by only the User password. The Master password previously set is still stored in the device but shall not be unlock
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed. Master password revision code set to the value in Master Password Revision Code field.

4.1.21. Security Unlock (F2h)

Feature	Security Mode feature set
Protocol	PIO data-out

Security unlock command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F2h							

Device register:

DEV *shall specify the selected device.*

Security unlock command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			

Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:
DEV *shall indicate the selected device.*
Status register:
BSY *will be cleared to zero indicating command completion*
DRDY *will be set to one.*
DF *(Device Fault) will be set to zero.*
DRQ *will be cleared to zero*
ERR *will be set to zero.*

Security unlock command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *The device shall return aborted if the device is in Frozen mode.*
This command transfers 512 bytes of data from the host. In Table of Idle command sector count register contents information, it defines the content of this information. If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.
If the Identifier bit is set to user then the device shall compare the supplied password with the stored User password. If the password compare fails then the device shall return command aborted to the host and decrements the unlock counter. This counter shall be initially set to five and shall decremented for each password mismatch when SECURITY UNLOCK and SECURITY ERASE UNIT commands shall be command aborted until a power-on reset or a hardware reset. SECURITY UNLOCK commands issued when the device is unlocked have no effect on the unlock counter.
Error Register:
ABRT *may be set to one if the device is not able to complete the action requested by the command*
Device register:
DEV *shall indicate the selected device.*
Status register:
BSY *will be cleared to zero indicating command completion*
DRDY *will be set to one.*
DF *(Device Fault) should be set to one if a device fault has occurred.*
DRQ *will be cleared to zero*
ERR *will be set to one if an Error register bit is set to one.*

4.1.22. Security Erase Prepare (F3h)

Feature	Security Mode feature set
Protocol	Non-data

Security erase prepare command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							

Sector Count	Na				
LBA Low	Na				
LBA Mid	Na				
LBA High	Na				
Device	obs	Na	obs	Na	Na
Command	F3h				

Device register:

DEV *shall specify the selected device.*

Security erase prepare command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:

DEV *shall indicate the selected device.*

Status register:

BSY *will be cleared to zero indicating command completion*

DRDY *will be set to one.*

DF *(Device Fault) will be set to zero.*

DRQ *will be cleared to zero*

ERR *will be set to zero.*

Security erase prepare command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *The SECURITY ERASE PREPARE command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command prevents accidental loss of data on the device. The device shall return aborted if the device is in Frozen mode.*

Error Register:

ABRT *shall be set to one if the device is in Frozen mode. ABRT may be set to one if the device is not able to complete the action requested by the command*

Device register

DEV *shall indicate the selected device.*

Status register

***BSY** will be cleared to zero indicating command completion*
***DRDY** will be set to one.*
***DF** (Device Fault) should be set to one if a device fault has occurred.*
***DRQ** will be cleared to zero*
***ERR** will be set to one if an Error register bit is set to one.*

4.1.23. Security Erase Unit (F4h)

Feature	Security Mode feature set
Protocol	PIO data-out

Security erase unit command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F4h							

Device register:
***DEV** shall specify the selected device.*

Security erase unit command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:
***DEV** shall indicate the selected device.*
Status register:
***BSY** shall be cleared to zero indicating command completion*
***DRDY** shall be set to one.*
***DF** (Device Fault) will be set to zero.*
***DRQ** shall be cleared to zero*
***ERR** shall be cleared to zero.*

Security erase unit command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *This command transfer 512 bytes of data from the host. In Table of Idle command for inputs information defines the content of this information. If the password does not match the password previously saved by the device, the device shall reject the command with command aborted.*

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command. If the device receives a SECURITY ERASE UNIT command without an immediately prior SECURITY ERASE PREPARE command, the device shall command abort the SECURITY ERASE UNIT command.

When Normal Erase mode is specified, the SECURITY ERASE UNIT command shall write binary zeroes to all user data areas. The Enhanced Erase mode is optional. When Enhanced Erase Mode is specified, the device shall write predetermined data patterns to all user areas. In Enhanced Erase mode, all previously written user data shall be overwritten, including sectors that are no longer in use due to reallocation.

This command shall disable the device Lock mode, however, the Master password shall still be stored internally within the device and may be reactivated later a new User password is set.

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Error Register

ABRT *shall be set to one if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, or if the data area is not successfully overwritten. ABRT may be set to one if the device is not able to complete the action requested by the command.*

Device register

DEV *shall indicate the selected device.*

Status register

BSY *will be cleared to zero indicating command completion*

DRDY *will be set to one. (DRDY set to one. This command shall be immediately preceded by a SECURITY ERASE PREPARE command.)*

DF *(Device Fault) should be set to one if a device fault has occurred.*

DRQ *will be cleared to zero*

ERR *will be set to one if an Error register bit is set to one.*

Security erase unit password information

Word	Content		
0	Control Word		
	Bit 0	Identifier	0=Compare User password
			1= Compare Master password
	Bit 1	Erase mode	0=Normal Erase
			1=Enhanced Erase
	Bit(15:2)	Reserved	

1-16	Password (32 Bytes)
17-255	Reserved

4.1.24. Security Freeze Lock (F5h)

Feature	Security Mode feature set
Protocol	Non-data

Security freeze lock for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	Na	Na	Na	Na	Na
Command	F5h							

Device register:

DEV *shall specify the selected device.*

Security freeze lock for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:

DEV *shall indicate the selected device.*

Status register:

BSY *shall be cleared to zero indicating command completion*

DRDY *shall be set to one.*

DF *(Device Fault) will be set to zero.*

DRQ *shall be cleared to zero*

ERR *shall be cleared to zero.*

Security freeze lock for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							

LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *The SECURITY FREEZE LOCK command shall set the device to Frozen mode. After command completion any other commands that update the device Lock mode shall be command aborted. Frozen mode shall be disabled by power-off or hardware reset. If SECURITY FREEZE LOCK shall be issued when the device in Frozen mode, the command executes and the device shall remain in Frozen mode.*

Command disabled by SECURITY FREEZE LOCK are:

SECUIRTY SET PASSWORD

SECURITY UNLOCK

SECURITY DISABLE PASSWORD

SECURITY ERASE PREPARE

SECURITY ERASE UNIT

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Error Register:

ABRT shall be set to one if the device is in locked mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Dvice register:

DEV *shall indicate the selected device.*

Status register:

BSY *will be cleared to zero indicating command completion*

DRDY *will be set to one.*

DF *(Device Fault) should be set to one if a device fault has occurred.*

DRQ *will be cleared to zero*

ERR *will be set to one if an Error register bit is set to one.*

4.1.25. Security Disable Password (F6h)

Feature	Security Mode feature set
Protocol	PIO data-out

Security disable password command for INPUTS information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F6h							

Device register:

DEV *shall specify the selected device.*

Security disable password command for NORMAL OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register:
DEV *shall indicate the selected device.*
Status register:
BSY *shall be cleared to zero indicating command completion*
DRDY *shall be set to one.*
DF *(Device Fault) will be set to zero.*
DRQ *shall be cleared to zero*
ERR *shall be cleared to zero.*

Security disable password command for ERROR OUTPUTS information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Description: *The SECURITY DISABLE PASSWORD command transfer 512 bytes of data from the host. In Table of Idle command sector count register contents information defines the content of this information. If the password selected by word 0 matches the password previously saved by the device, the device shall disable the Lock mode. This command shall not change the Master password. The Master password shall be reactivated when a User password if set. The device shall return aborted if the device is in Locked mode, or device is in Frozen mode.*
Error Register:
ABRT *may be set to one if the device is not able to complete the action requested by the command.*
Device register:
DEV *shall indicate the selected device.*
Status register:
BSY *will be cleared to zero indicating command completion*
DRDY *will be set to one. (Device shall be in Unlocked mode.)*
DF *(Device Fault) should be set to one if a device fault has occurred.*
DRQ *will be cleared to zero*
ERR *will be set to one if an Error register bit is set to one.*

Security disables password command content

Word	Content
0	Control Word Bit 0 Identifier 0=Compare User password 1= Compare Master password Bit(15:1) Reserved
1-16	Password (32 Bytes)
17-255	Reserved

Appendix A Ordering Information

Part Number List:

1. APRO MLC micro SATA II Flash Module Part Number

Part number list – Vertical type Standard Form Factor		
Photo	**Capacity**	**Operating temperature supports 0˚ C~ 70˚ C**
	4GB	SPMSF004G-JDCMM-VS(-F)
	8GB	SPMSF008G-JDCMM-VS(-F)
	16GB	SPMSF016G-JDCMM-VS(-F)
	32GB	SPMSF032G-JDCMM-VS(-F)
	64GB	SPMSF064G-JDCMM-VS(-F)
	128GB	SPMSF128G-JDCMM-VS(-F)

Remark:

-F: optional item power pin-7 with fuse

Part Number Decoder:

X1 X2 X3 X4 X5 X6 X7 X8 X9 – X11 X12 X13 X14 X15 – Y1 Y2 F

X1 : **Grade**

S : Standard Grade – operating temp. 0º C ~ 70 º C

X2 : **The material of case**

P : Plastic casing

X3 X4 X5 : **Product category**

MSF : micro SATA flash module

X6 X7 X8 X9 : **Capacity**

004G:	4GB	**32G:**	32GB
008G:	8GB	**64G:**	64GB
016G:	16GB	**128G:**	128GB

X11 : **Controller**

J : JMicron (HERMES Series)

X12 : **Controller version**

A, B, C……D

X13 : **Controller grade**

C : Commercial grade

X14 : **Flash IC**

M : Micron NAND Flash IC

X15 : **Flash IC grade / Type**

M : MLC-NAND flash IC

Y1 Y2 : **MSF orient only**

VS : Vertical type standard form factor

F : **Reserved for specific requirement**

F : Power pin-7 with fuse

Appendix B Limited Warranty

APRO warrants your micro SATA II Flash (MSF) Module against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

Warranty Period:

- ***SPMSFxxxG-JDCMM-VS(-F)*** ***2 years***

The warranty period is able to extend. Please contact with APRO and / or Your APRO distributor for more information.