



November 2008

Product Specification Industrial Secure Digital (SD) Card

– IAISI Series –

Doc-No: 100-WPSPDC-01V0

INDUSTRIAL *Secure Digital (SD) Memory Card*



This document is for information use only and is subject to change without prior notice. APRO Co., Ltd. Assumes no responsibility for any errors that may appear in this document, nor for incidental or consequential damages resulting from the furnishing, performance or use of this material. No part of this document may be reproduced, transmitted, transcribed, stored in a retrievable manner or translated into any language or computer language, in any form or by any means, electronic, mechanical, magnetic, optical, chemical, manual or otherwise, without the prior written consent of an officer of APRO Co., Ltd..

All parts of the APRO documentation are protected by copyright law and all rights are reserved.

APRO and the APRO logo are registered trademarks of APRO Co., Ltd.

Product names mentioned herein are for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

© 2009 APRO Corporation. All rights reserved.

Revision History

<i>Rev.</i>	<i>Description</i>	<i>Update</i>
<i>1.0</i>	<i>Initial release</i>	<i>2009/3/17</i>

CONTENTS

1. INTRODUCTION	3
1.1. SCOPE	4
1.2. SYSTEM FEATURES	4
1.3. SD CARD STANDARD	4
1.4. FUNCTIONAL DESCRIPTION	4
1.4.1. TECHNOLOGY INDEPENDENCE	5
1.4.2. WEAR LEVELING	5
1.4.3. FLASH MEMORY ACCESS	5
1.4.4. MANAGEMENT OF FLASH MEMORY DEFECTS	5
1.4.5. ERROR RECOVERY	5
1.4.6. POWER MANAGEMENT	6
1.4.7. DUAL BLOCK MODE	6
1.4.8. SD/MMC MEMORY CARD INTERFACE	6
1.4.9. CONTENT PROTECTION FOR RECORDABLE MEDIA	6
1.4.10. COPYRIGHT PROTECTION	7
2. PRODUCT SPECIFICATIONS	8
2.1. SYSTEM ENVIRONMENTAL SPECIFICATIONS	8
2.2. SYSTEM POWER REQUIREMENTS	8
2.3. SYSTEM PERFORMANCE	8
2.4. SYSTEM RELIABILITY	8
2.5. PHYSICAL SPECIFICATIONS	9
2.6. CAPACITY SPECIFICATIONS	11
3. SD MEMORY CARD INTERFACE DESCRIPTION	12

3.1. PHYSICAL DESCRIPTION	12
3.1.1. PIN ASSIGNMENTS IN INDUSTRIAL GRADE SD CARD MODE	12
3.1.2. PIN ASSIGNMENTS IN SPI MODE.....	13
3.2. SD BUS TOPOLOGY	14
3.3. SPI BUS TOPOLOGY	16
4. ELECTRICAL SPECIFICATIONS	18
4.1. ABSOLUTE MAXIMUM RATINGS.....	18
4.2. RECOMMENDED OPERATING CONDITIONS.....	18
4.3. DC CHARACTERISTICS.....	19
4.4. AC CHARACTERISTICS.....	19
4.4.1. BUS SIGNAL LEVELS	19
4.4.2. BUS TIMING (SD DEFAULT MODE).....	20
4.4.3. BUS TIMING (SD HIGH-SPEED MODE).....	21
5. SD MEMORY CARD PROTOCOL DESCRIPTION	22
5.1. SD BUS PROTOCOL	22
6. SPI PROTOCOL DEFINITION.....	25
6.1. SPI BUS PROTOCOL	25
6.1.1. DATA READ.....	25
6.1.2. DATA WRITE	27
APPENDIX A. ORDERING INFORMATION	29
APPENDIX B. LIMITED WARRANTY.....	30

1. Introduction

The APRO Industrial Grade Secure Digital (SD) Memory Card is NAND-SLC Flash based memory card that is specifically designed to meet the security, performance and environmental requirements of some significant applications such like networking, telecommunications and data-communications, mobile & embedded computing, medical instruments and industrial computing applications. The APRO Industrial Grade SD Memory Card includes a copyright protection that complies with the security of the SDMI standard, and the physical form-factor, pin assignment and data transfer protocol are forward compatible with SD memory Card, with some additions.

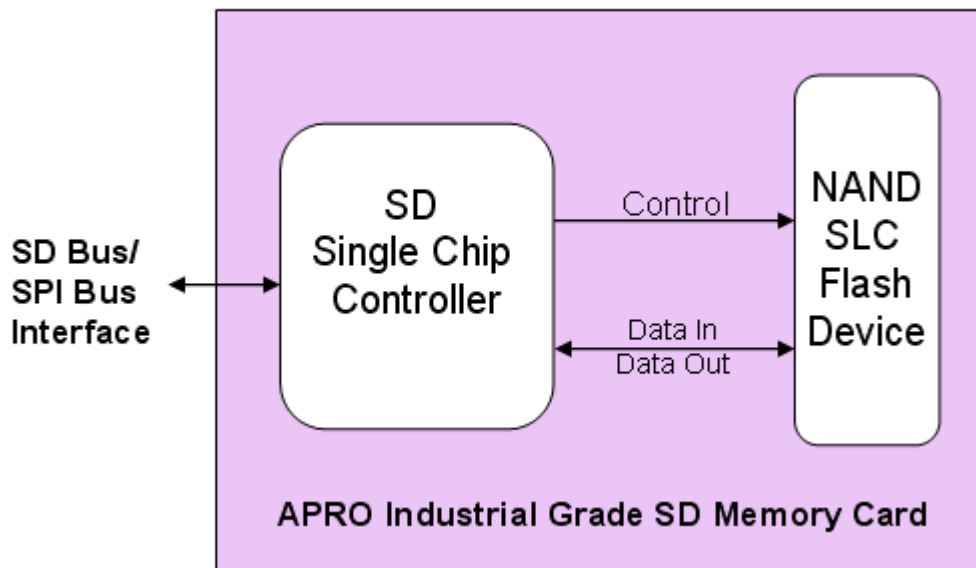


Figure 1: Industrial Grade SD Memory Card Block Diagram

1.1. **Scope**

This document describes the key features and specifications of APRO Industrial Grade SD Memory Card, as well as the information required to interface this product to a host system.

1.2. **System Features**

- NAND type SLC Flash technology
- Fully compatible with SD Card Specification Version 2.0
- 9 exposed contacts on one side
- Supports industrial grade operating temperature -40°C to -85°C
- Capacity from 128MB to 2GB
- SD Card protocol compatible
- Supports SD mode and SPI mode
- Copyright Protection Mechanism-Complies with highest security of SDMI standard
- Write protect feature using mechanical switch
- Performance up to 19MB/sec

1.3. **SD Card Standard**

APRO Industrial Grade SD Memory Cards are fully compatible with the following SD physical Layer Specification standard:

SD Memory Card Specifications, Part 1, Physical Layer Specification, Version 2.00

This specification may be obtained from:

SD Card Association
53 Muckelemi St.
P.O. Box 189
San Juan Bautista, CA 95045-0189
USA
Phone : 831-623-2107
Fax : 831-623-2248
<http://www.sdcard.org>

1.4. **Functional Description**

APRO Industrial Grade SD Cards contain a high level and intelligent subsystem as shown in Figure 1. This intelligent SD memory card controller manages interfaced protocols and data storage and retrieval as well as Error Correction Code (ECC) algorithms, defect handling and diagnostics, power management related functions. For SD card, Content Protection for Recordable Media related function is also included.

1.4.1. Technology Independence

The 512-byte sector size of the SD Memory Card is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues a Read or Write command to the SD Memory Card. This command contains the address and the number of sectors to write/read. The host software then waits for the command to complete. The host software does not get involved in the details of how the flash memory is erased, programmed or read. This is extremely important as flash devices are expected to get more and more complex in the future. Since the SD Memory Card Titans Series uses an intelligent on-board controller, the host system software will not require changing as new flash memory evolves. In other words, systems that support the SD Memory Card today will be able to access future APRO cards built with new flash technology without having to update or change host software.

1.4.2. Wear Leveling

Wear Leveling is an intrinsic part of the Erase Pooling functionality of APRO SD Memory Cards using NAND memory. The WEAR LEVELING command is supported to ensure the best of flash memory endurance capability.

1.4.3. Flash Memory Access

To write or read a sector (or multiple sectors), the master (host device) simply issues a read or a write command set to the SD Memory Card Controller. The command set contains the address and related information about the access characteristics. The master (host device) does not get involved in the details of how the flash memory is erased, programmed or read.

1.4.4. Management of Flash Memory Defects

APRO Industrial SD Memory Card also contains a sophisticated defect and error management system. The SD Memory Card controller does a read after write under margin conditions to verify that the data is written correctly (except in the case of write pre-erased sectors). In case that a bit is found to be defective, the SD Memory Card Controller replaces this bad bit with a spare bit within the sector header. If necessary, the SD Memory Card Controller will even replace the entire sector with a spare sector. This is completely transparent to the master (host device) and does not consume any user data space.

1.4.5. Error Recovery

In the rare case a read error does occur, the SD Memory Card Controller has an innovative algorithm to recover the data. The last line of defense is to employ a powerful ECC to correct the data. If ECC is used to recover data, defective bits are replaced with spare bits to ensure they do not cause any future problems. For the SD Memory Card Controller, it could correct up to 8 bits data errors per 528 bytes data or 15 bits data errors per 539 bytes data automatically.

1.4.6. Power Management

A power saving feature of the SD Memory Card Controller is automatic entrance and exit from sleep mode. Upon completion of an operation, the SD Memory Card Controller will enter the sleep mode to conserve power if no further commands are received within X seconds, where X is programmable by software. The master does not have to take any action for this to occur. The SD Memory Card Controller is in sleep mode except when the host is accessing it, thus conserving power. Any command issued by the master to the SD Memory Card Controller will cause it to exit sleep mode and response to the master.

1.4.7. Dual Block Mode

In order to provide high performance read/write operation, the SD Memory Card Controller provides dual block mode operation scheme, which would be able to operate two 8-bit flash memories concurrently. When dual block mode is enabled, the SD Memory Card Controller will operate two selected flash memories as a pseudo flash memory, thus saving lots of operating time and providing much better performance compared to single 8-bit flash memory.

1.4.8. SD/MMC Memory Card Interface

The SD Memory Card Controller provides four alternative communication protocols: SD, MMC, SPI under SD, and SPI under MMC. After deciding SD or MMC card is manufactured, applications can choose between SD and SPI under SD mode or between MMC and SPI under MMC mode automatically. Mode selection is transparent to the hosts. The SD/MMC Memory Card Controller automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. Therefore, applications that use only one communication mode do not have to be aware of the others.

1.4.9. Content Protection for Recordable Media

The Content Protection for Recordable Media (CPRM) technology applied by SD card is designed to meet the following criteria:

- It meets the content owners' requirements for robustness and system renewability
- It is applicable for both audio and video content
- It is equally suitable for implementation on PCs and CE devices
- It is applicable to different media type

The system is based on the following technical elements

- Key management for interchangeable media
- Content encryption
- Media based renewability

1.4.10. Copyright Protection

A detailed description of the Copyright Protection mechanism and related security SD Card commands can be found in the SD Card Security Specification document from the SD Card Association. All Industrial Grade SD Card security related commands operate in the data transfer mode.

As defined in the SDMI specification, the data content that is saved in the card is saved already encrypted and it passes transparently to and from the card. No operation is done on the data and there is no restriction to read the data at any time. Associated with every data packet (song, for example) that is saved in the unprotected memory there is a special data that is saved in a protected memory area. For any access (any Read, Write or Erase command) from/to the data in the protected area. For an authentication procedure is done between the card and the connected device, either the LCM (PC for example) or the PD (portable device, such as SD player). After the authentication process passes, the card is ready to accept or give data from/to the connected device. While the card is in the secured mode of operation (after the authentication succeeded) the argument and the associated data that is sent to the card or read from the card are encrypted. At the end of the Read, Write or Erase operation, the card gets out automatically of its secured mode.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 1: Environmental Specification

Temperature	Operating: Non-operating:	-40°C ~ +85°C -65°C ~ +100°C
Humidity	Operating & Non-operating:	25% ~ 95% non-condensing
Vibration	Operating & Non-operating:	15G compliance to MIL-STD-810F
Shock	Operating & Non-operating:	1500 G compliance to MIL-STD-810F
ESD Protection	Contact Pads : Non Contact Pads Area :	±4kV, Human body model according to ANSI EOS/ESD-S5.1-1998 ±8kV (coupling plane discharge) ±15kV (air charge), Human body model per IEC61000-4-2
Altitude	Operating & Non-operating:	8,000 feet

2.2. System Power Requirements

Table 2: System Power Requirement

DC Input Voltage (VCC)	2.7V ~ 3.6V
Reading Mode :	68 mA(Max.)
Writing Mode :	80 mA (Max.)
Standby Mode :	450μ A(Typ.)

2.3. System Performance

Table 3: System Performances

Sequential Read	19 MB/sec
Sequential Write	9.3 MB/sec
Average Access Time	1.0 ms (estimated)

Note:

- (1) All values quoted are typically at 25°C and nominal supply voltage.
- (2) The Max. Performance was tested by HDBENCHG MARK/1GB SD Card
- (3) The performance would be different for the system's configuration

2.4. System Reliability

Table 4: System Reliability

Durability	10,000 inserting cycles
Bending	10N
Torque	0.15 N +/- 2.5 deg.
Drop Test	1.5M free fall
WP Switch Cycle	1,000 cycles @ slide force 0.4N to 5N
Wear-leveling Algorithms	Dynamic wear-leveling algorithms

MTBF	> 2,000,000 hours
ECC Technology	Correcting up to 8 bits data errors per 528 bytes data or 15 bits data errors per 539 bytes data automatically
Endurance	> 2,000,000 cycles logically contributed by dynamic wear-leveling and advanced bad sector management algorithms
Data Reliability	< 1 non-recoverable error in 10^{14} bits read
Data Retention	10 years

2.5. Physical Specifications

Refer to Table 5 and see Figure 2 ~ Figure 4 for SD Memory Card physical specifications and dimensions.

Table 5 : Physical Specifications

Industrial SD Memory Card	
Length:	24.00±0.10mm(0.95 in)
Width:	32.00±0.10mm(1.26 in)
Thickness:	2.1±0.15mm(0.08 in)
Weight:	2.0g(0.07oz) typical

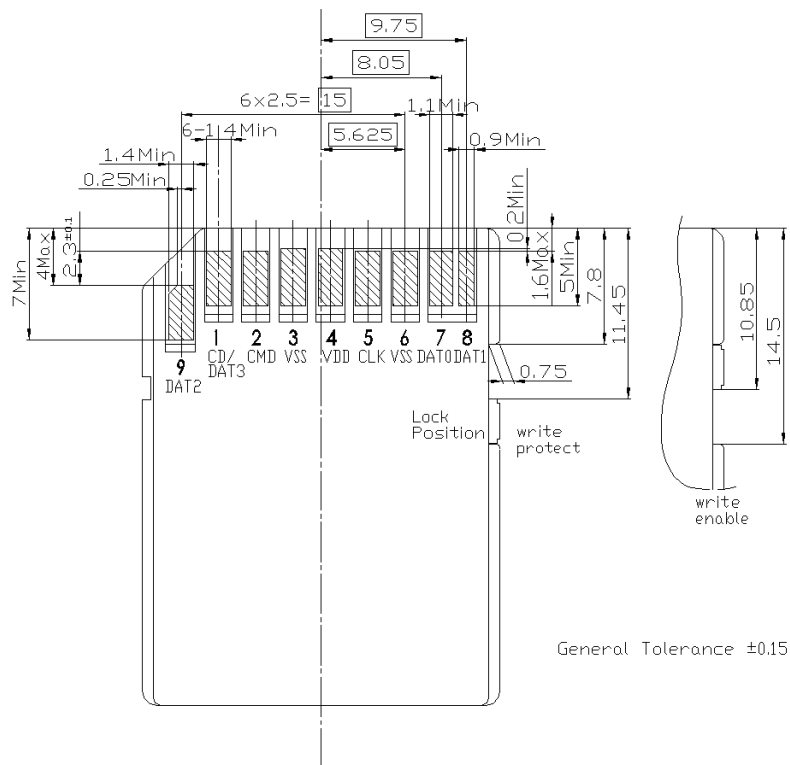


Figure 2: SD Memory Card Dimensions (1 out of 3)

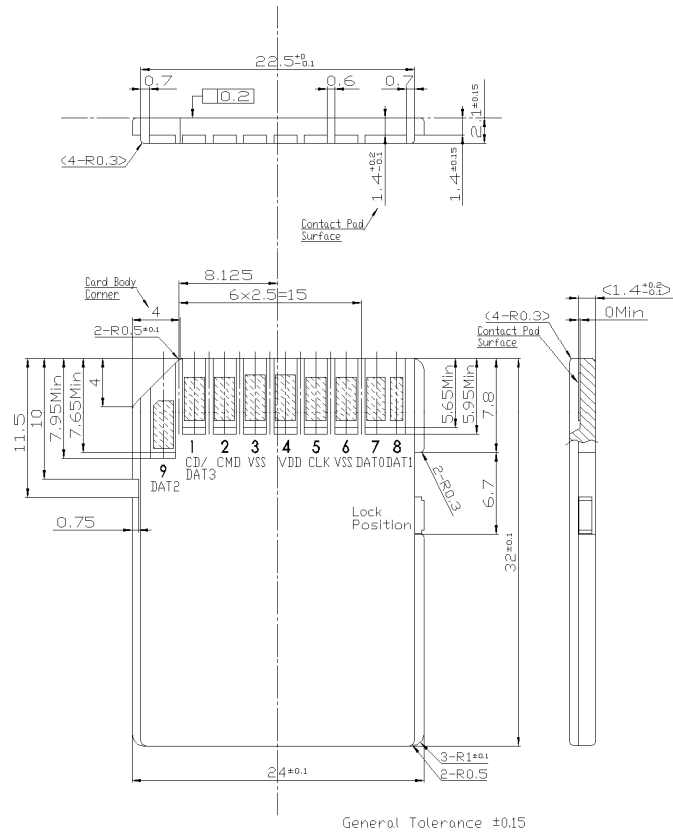


Figure 3: SD Memory Card Dimensions (2 out of 3)

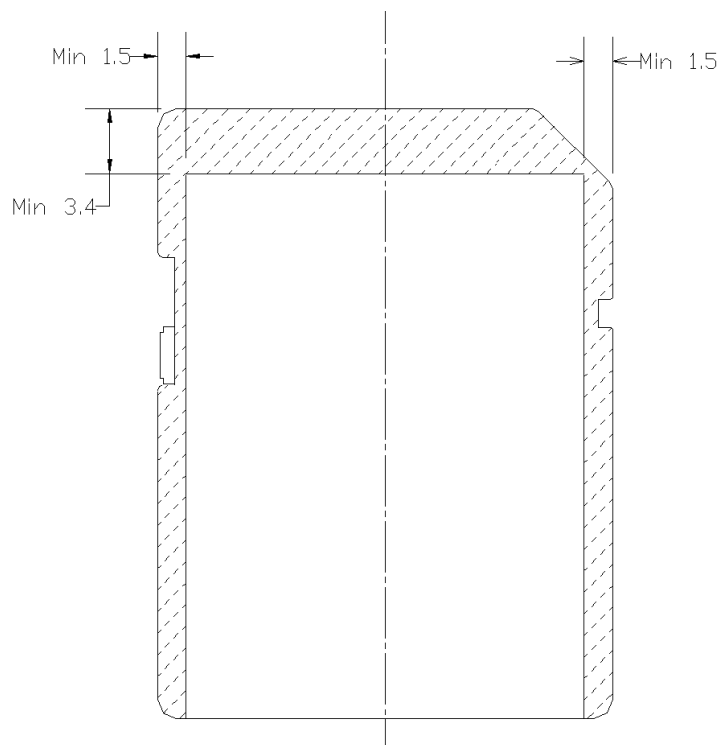


Figure 4: SD Memory Card Dimensions (3 out of 3)

2.6. Capacity Specifications

APRO Industrial SD Memory Card is built-in mainly Samsung NAND Type SLC Flash memory chips. The Table 6 shows the equipollent part number of applied Samsung Flash memory chips for each card.

Table 6: Card Configuration vs. Samsung NAND SLC part number

Card Capacity	Samsung SLC Flash Memory Part Number * Q'TY
128MB	K9F1G08U0B-PXB0 (1Gb) or equipollent * 1
256MB	K9F2G08U0A-PXB0 (2Gb) or equipollent * 1
512MB	K9F4G08U0A-PXB0 (4Gb) or equipollent * 1
1GB	K9K8G08U0A-PXB0 (8Gb) or equipollent * 1
2GB	K9WAG08U1A-PXB0 (16Gb) or equipollent * 1

The table 7 shows the specific capacity for the various models and the default number of heads, sectors/track and cylinders.

Table 7: Model Capacity

Unformatted Capacity	Default Cylinder	Default Head	Default Sector	Default CHS Capacity
128MB	15	255	63	123,379,200
256MB	30	255	63	246,758,400
512MB	61	255	63	501,742,080
1GB	123	255	63	1,011,709,440
2GB	244	255	63	2,006,968,320

3. SD Memory Card Interface Description

3.1. Physical Description

APRO Industrial Grade SD Memory Card has nine exposed contacts on one side (see Figure 1 and Figure 2). The host is connected to the SD Card using a dedicated 9-pin connector.

3.1.1. Pin Assignments in Industrial Grade SD Card Mode

The signal/pin assignments and definitions in SD Card Mode are listed in below Table 8.

Table 8: SD Bus Mode Pin Definition

Pin #	Name	Type1	SD Description
1	CD/DAT32	I/O3	Card Detect/Data Line [Bit 3]
2	CMD	I/O	Command/Response
3	VSS1	S	Supply voltage ground
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	VSS2	S	Supply voltage ground
7	DAT0	I/O	Data Line [Bit 0]
8	DAT1	I/O	Data Line [Bit 1]
9	DAT2	I/O	Data Line [Bit 2]

- Notes:
- 1) S=power supply; I=input; O=output using push-pull drivers.
 - 2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after the SET_BUS_WIDTH command. It is the responsibility of the host designer to connect external pullup resistors to all data lines even if only DAT0 is to be used. Otherwise, non-expected high current consumption may occur due to the floating inputs of DAT1 & DAT2 (in case they are not used).
 - 3) After power up, this line is input with 50Kohm(+/-20Kohm) pull-up (can be used for card detection or SPI mode selection). The pull-up may be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

3.1.2. Pin Assignments in SPI Mode

Table 9 lists the pin assignments and definitions in SPI Mode

Table 9 : SPI Bus Mode Pin Definition

Pin #	Name	Type1	SPI Description
1	CS	I	Chip Select (Active low)
2	Data In	I	Host to Card Commands and Data
3	VSS1	S	Supply Voltage Ground
4	VDD	S	Supply Voltage
5	CLK	I	Clock
6	VSS2	S	Supply Voltage Ground
7	Data Out	O	Card to Host Data and Status
8	RSV(2)	I	Reserved
9	RSV(2)	I	Reserved

NOTES: 1) S=power supply; I=input; O=output.
2) The 'RSV' pins are floating inputs. It is the responsibility of the host designer to connect external pullup resistors to those lines. Otherwise non-expected high current consumption may occur due to the floating inputs.

Each card has a set of information registers (refer to Table 10).

Table 10 : Industrial Grade SD Card Registers

Name	Width	Description
CID	128	Card identification number: individual card number for identification.
RCA1	16	Relative card address: local system address of a card, dynamically suggested by the card and approved by the host during initialization.
CSD	128	Card specific data: information about the card operation conditions.
SCR	64	SD Configuration Register: information about the SD Card's special features capabilities.
OCR	32	Operation Condition Register

NOTE: 1) The RCA register is not available in SPI Mode.

The host may reset the cards by switching the power supply off and on again. The card has its own power-on detection circuitry which puts the card into an idle state after the power-on. The card can also be reset by sending the GO_IDLE (CMD0) command.

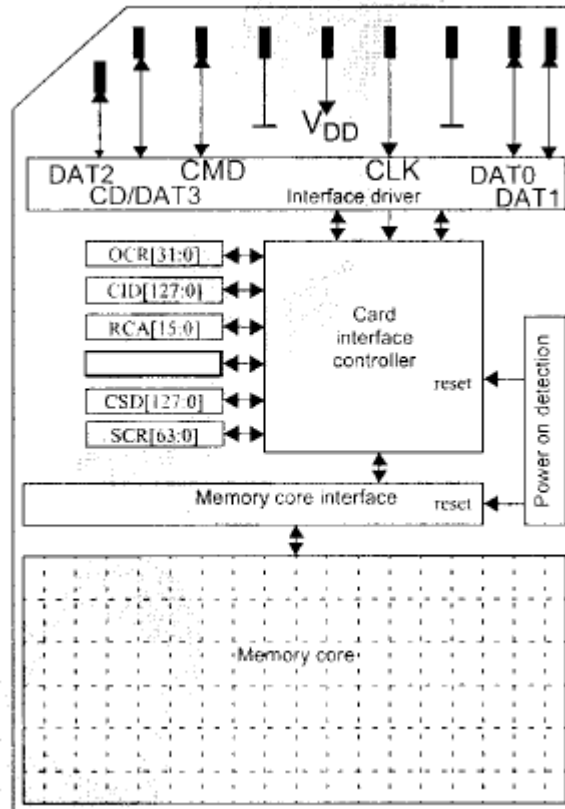


Figure 5 : Industrial Grade SD Card Architecture

3.2. SD Bus Topology

The SD bus has six communication lines and three supply lines:

- **CMD**—Command is a bi-directional signal. (Host and card drivers are operating in push pull mode.)
- **DAT0-3**—Data lines are bi-directional signals. (Host and card drivers are operating in push pull mode.)
- **CLK**—Clock is a host to cards signal. (CLK operates in push pull mode.)
- **VDD**—VDD is the power supply line for all cards.
- **VSS [1:2]**—VSS are two ground lines.

Figure 6 shows the bus topology of several cards with one host in SD Bus mode.

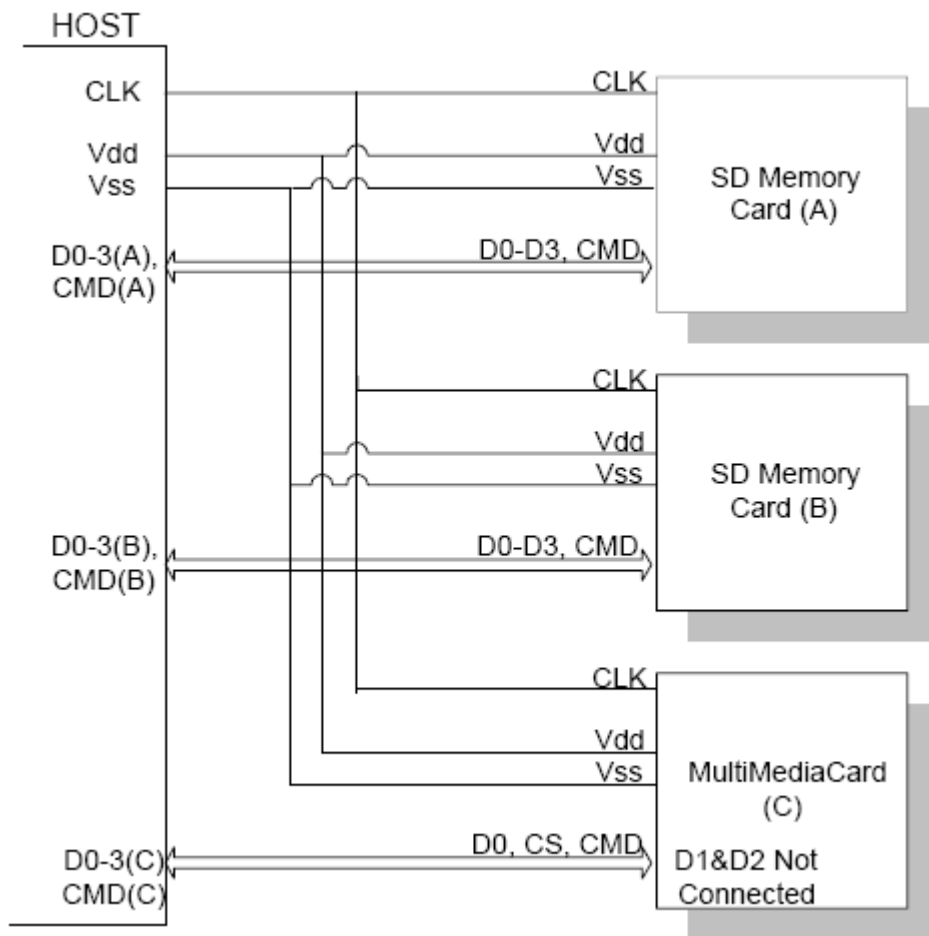


Figure 6 : Industrial Grade SD Card System Bus Topology

During the initialization process, commands are sent to each card individually, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent to each card individually. However, to simplify the handling of the card stack, after initialization, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.

The SD Bus allows dynamic configuration of the number of data lines. After power-up, by default, the Industrial Grade SD Card will use only DAT0 for data transfer. After initialization, the host can change the bus width (number of active data lines). This feature allows an easy trade off between hardware cost and system performance.

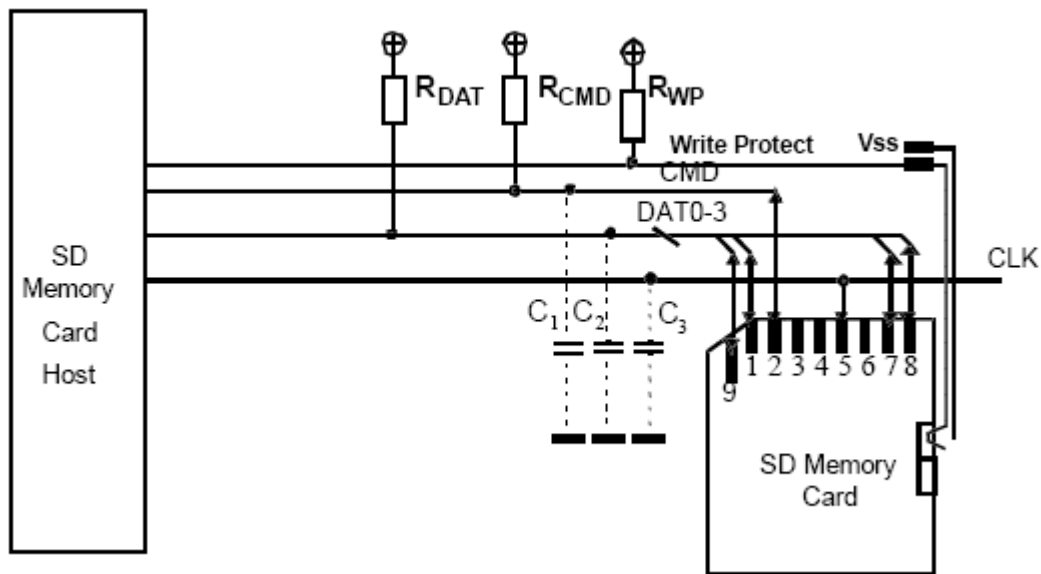


Figure 7 : Bus Circuitry Diagram

R_{DAT} and R_{CMD} are pull-up resistors protecting the CMD and the DAT line against bus floating when no card is inserted or when all card drivers are in a hi-impedance mode. R_{WP} is used for the Write Protect Switch.

3.3. SPI Bus Topology

The Industrial Grade SD Card SPI interface is compatible with SPI hosts available on the market. As any other SPI device, the SD Card SPI channel consists of the following four signals:

- **CS**—Host to card Chip Select signal.
- **CLK**—Host to card clock signal.
- **Data In**—Host to card data signal.
- **Data Out**—Card to host data signal.

Another SPI common characteristic implemented in the Industrial Grade SD Card is byte transfers. All data tokens are multiples of 8-bit bytes and always byte aligned to the CS signal. The SPI standard defines the physical link only and not the complete data transfer protocol. In SPI Bus mode, the Industrial Grade SD Card uses a subset of the SD Card protocol and command set.

The Industrial Grade SD Card identification and addressing algorithms are replaced by a hardware Chip Select (CS) signal. A card (slave) is selected, for every command, by asserting (active low) the CS signal (see Figure 7). The CS

signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception is card programming time. At this time the host can de-assert the CS signal without affecting the programming process.

The bi-directional CMD and DAT lines are replaced by uni-directional dataIn and dataOut signals. This eliminates the ability of executing commands while data is being read or written. An exception is the multi read/write operations. The Stop Transmission command can be sent during data read. In the multi block write operation a Stop Transmission token is sent as the first byte of the data block.

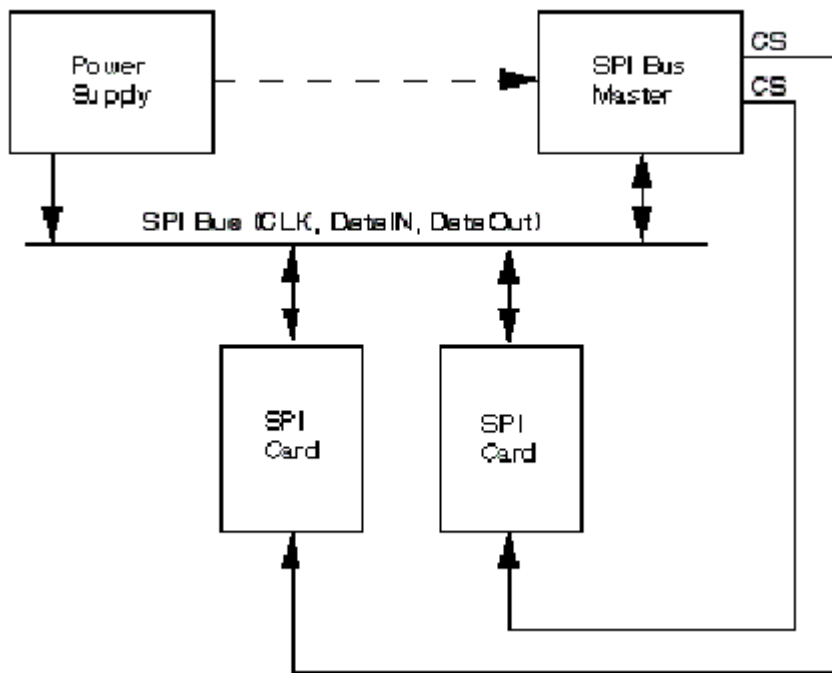


Figure 8 : Industrial Grade SD Card Bus System

4. Electrical Specifications

The following tables define all DC Characteristics and AC Characteristics for the Industrial Grade SD Memory Card.

4.1. Absolute Maximum Ratings

Table 11 describes Absolute Maximum Ratings of Industrial Grade SD Memory Card.

Table 11 : Absolute Maximum Ratings Parameter Value

SYMBOL	PARAMETER	RATING	UNITS
V _{CC}	Power supply relative to V _{SS}	1.65 to 1.95, 2.7 to 3.6	V
V _{IN}	Input voltage relative to V _{SS}	-0.3 to 3.9	V
T _{STG}	Storage temperature	-65 to 100	°C
T _{OP}	Operation temperature	-40 to 85	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the optional sections of this datasheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4.2. Recommended Operating Conditions

Table 12 describes Recommended Operating Conditions of Industrial Grade SD Memory Card.

Table 12 : Recommended Operating Conditions Parameter Value

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V _{CCH}	Power supply voltage (high voltage range)	2.7	3.3	3.6	V
V _{CCL}	Power supply voltage (low voltage range)	1.65	1.8	1.95	V
V _{SS}	Power supply voltage	-0.5	0	0.5	V
T _A	Recommended operating ambient temperature	-40	-	85	C

4.3. DC Characteristics

Table 13 describes DC Characteristics of Industrial Grade SD Memory Card.

Table 13 : DC Characteristics Parameter Value

Symb ol	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IL}	Input low voltage		V _{SS} -0.3	-	0.25V _{CCH} / 0.3V _{CCL}	V
V _{IH}	Input high voltage		0.625V _{CCH} / /0.7V _{CCL}	-	V _{CC} +0.3	V
V _{OL}	Output low voltage	I _{OL} =100 μA @ V _{CC_min}	-	-	0.125V _{CCH} /0. 2	V
V _{OH}	Output high voltage	I _{OH} =-100 μA @ V _{CC_min}	0.75V _{CCH} / V _{CCL} -0.2	-	-	V
I _{IN}	Input leakage current	V _{IN} =V _{CC} or 0	-10	+/-1	10	μA
I _{OUT}	Tri-state output leakage current		-10	+/-1	10	μA
I _{STBY}	Standby current	@ Clock Stop	-	60	80	μA
I _{OP}	Operation current	3.3V @ Write	-	-	25	mA
		3.3V @ Read	-	-	25	mA
I _{OP}	Operation current	1.8V @ Write	-	-	25	mA
		1.8V @ Read	-	-	25	mA

4.4. AC Characteristics

4.4.1. Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage (see Figure 9).

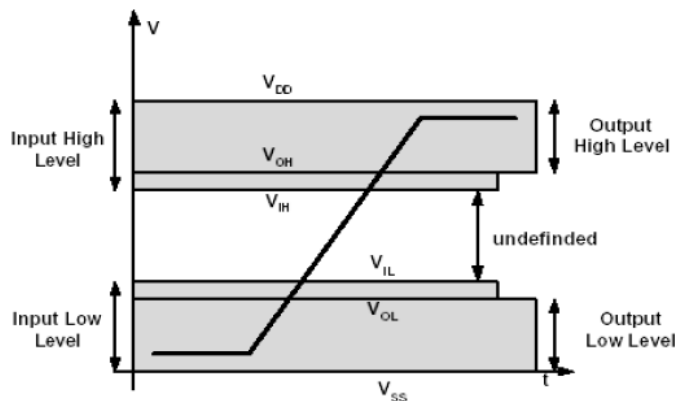


Figure 9 : Bus Signal Levels

To meet the requirements of the JEDEC specification JESD8-1A, the card input and output voltages shall be within the specified ranges in Table 14 for any VDD of the allowed voltage range.

Table 14 : Input and Output Voltages

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output HIGH voltage	VOH	0.75*VDD		V	IOH=-100μA @VDD(min.)
Output LOW voltage	VOL		0.125*VDD	V	IOL=100μA @VDD(min.)
Input HIGH voltage	VIH	0.625*VDD	VDD+0.3	V	
Input LOW voltage	VIL	VSS-0.3	0.25*VDD	V	

4.4.2. Bus Timing (SD Default Mode)

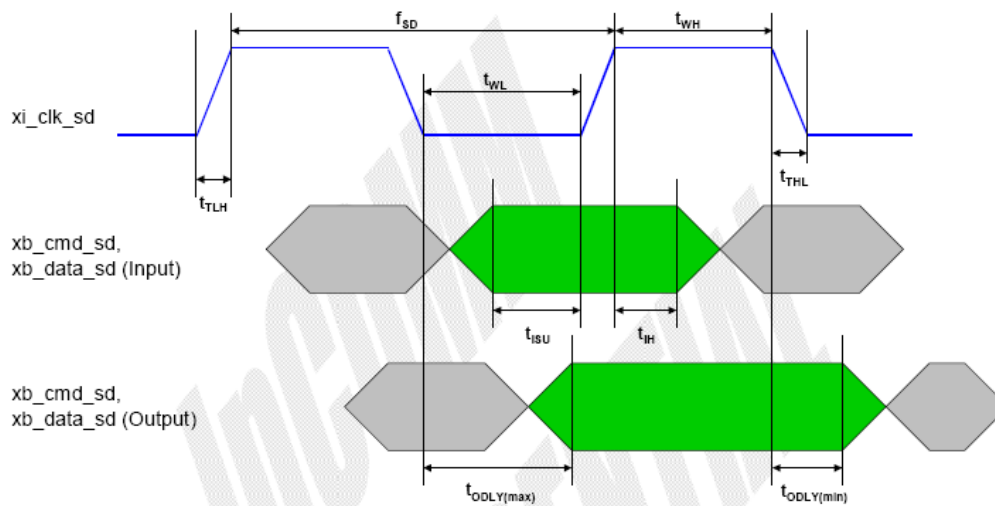


Figure 10 : Timing Diagram of SD Default Mode Bus Timing

Table 15 : SD Default Mode Bus Timing Parameter Value

SYMBOL	PARAMETER	MIN	MAX	UNIT	Note
f _{SD}	SD clock frequency	0	25	MHz	
t _{WL}	Clock low time	10	-	ns	
t _{WH}	Clock high time	10	-	ns	
t _{TLH}	Clock rise time	-	10	ns	
t _{THL}	Clock fall time	-	10	ns	
t _{ISU}	Input setup time	5	-	ns	
t _{IH}	Input hold time	5	-	ns	
t _{ODLY}	Output delay time	0	14	ns	

4.4.3. Bus Timing (SD High-speed Mode)

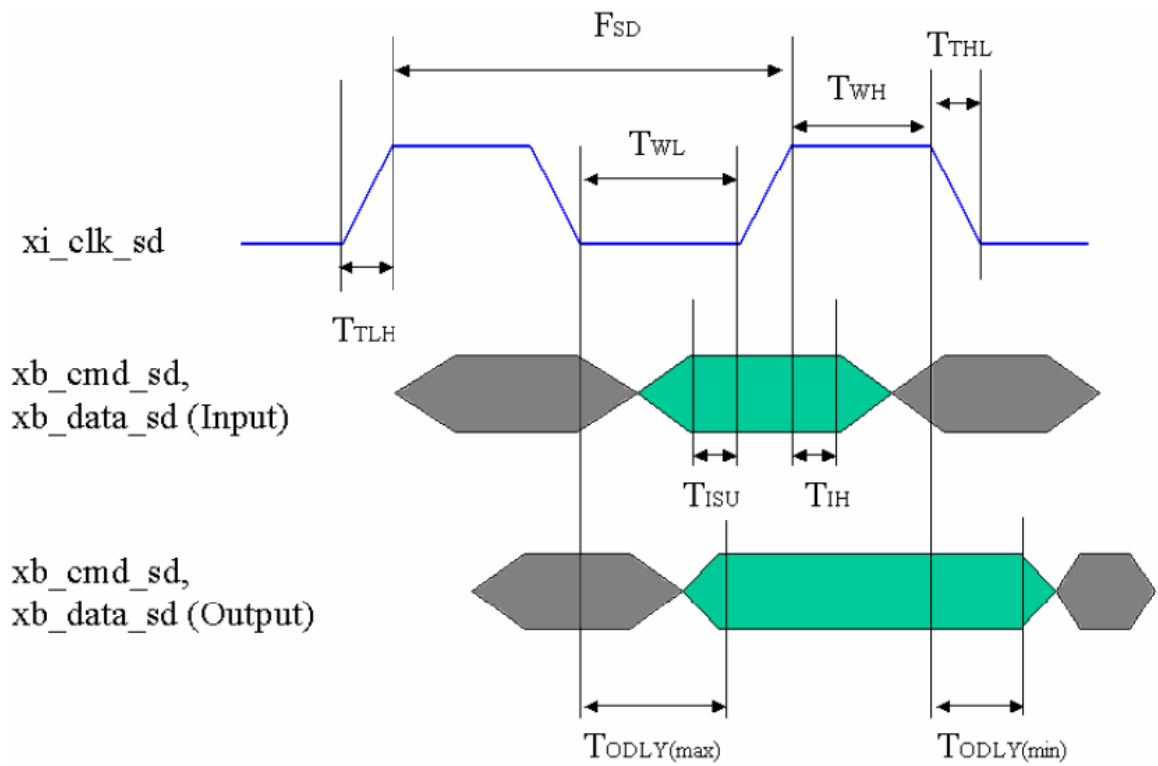


Figure 11 : Timing Diagram of SD High-Speed Mode Bus Timing

Table 16 : SD High-Speed Mode Bus Timing Parameter Value

SYMBOL	PARAMETER	MIN	MAX	UNIT	Note
f_{SD}	SD clock frequency	0	50	MHz	
t_{WL}	Clock low time	7	-	ns	
t_{WH}	Clock high time	7	-	ns	
t_{TLH}	Clock rise time	-	3	ns	
t_{THL}	Clock fall time	-	3	ns	
t_{ISU}	Input setup time	6	-	ns	
t_{IH}	Input hold time	2	-	ns	
t_{ODLY}	Output delay time	-	14	ns	
t_{OH}	Output hold time	2.5	-	ns	

5. SD Memory Card Protocol Description

5.1. SD Bus Protocol

Communication over the SD bus is based on command and data bit streams, which are initiated by a start bit and terminated, by a stop bit:

- **Command** — A command is a token that starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- **Response** — A response is a token that is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- **Data** — Data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

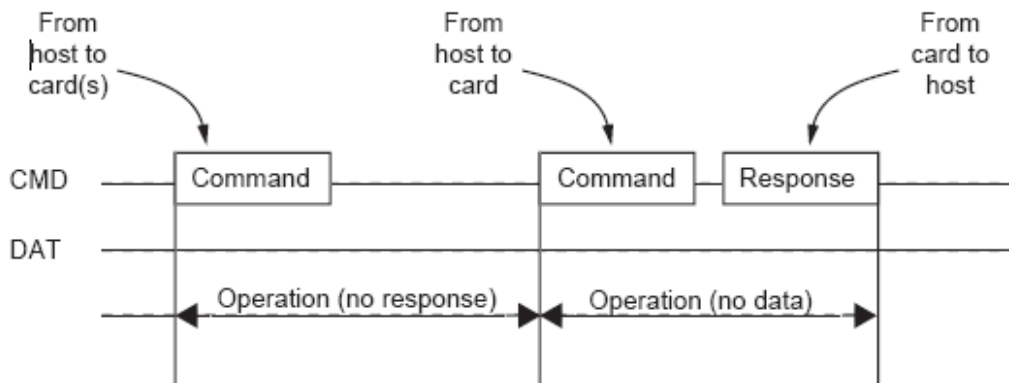


Figure 12 : “No Response” and “No Data” Operations

Card addressing is implemented using a session address that is assigned to the card during the initialization phase. The basic transaction on the SD bus is the command/response transaction (see Figure 12). This type of bus transaction transfers their information directly within the command or response structure. In addition, some operations have a data token.

Data transfers to/from the Industrial Grade SD Card are done in blocks. Data blocks are always followed by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode is better for faster write operation. A multiple block transmission is terminated when a stop command follows on the CMD line. Data transfer can be configured by the host to use single or multiple data lines (as long as the card supports this feature).

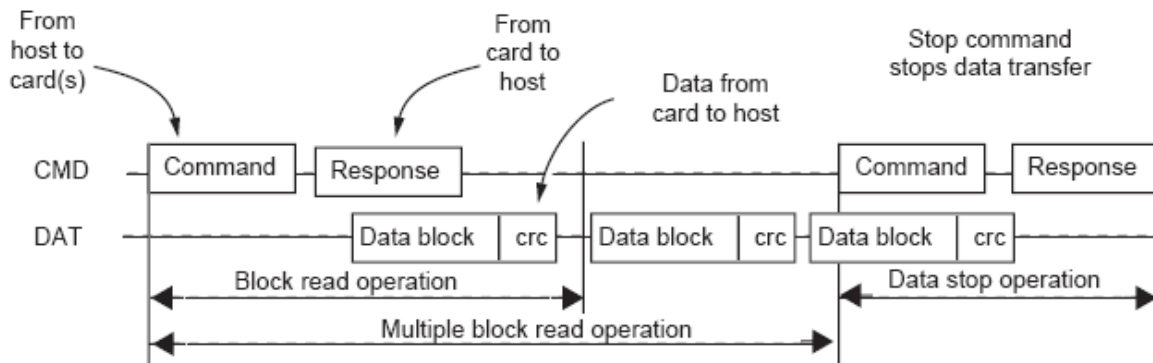


Figure 13 : Multiple Block Read Operation

The block write operation uses a simple busy signaling of the write operation duration on the DAT0 data line (see Figure 14) regardless of the number of data lines used for transferring the data.

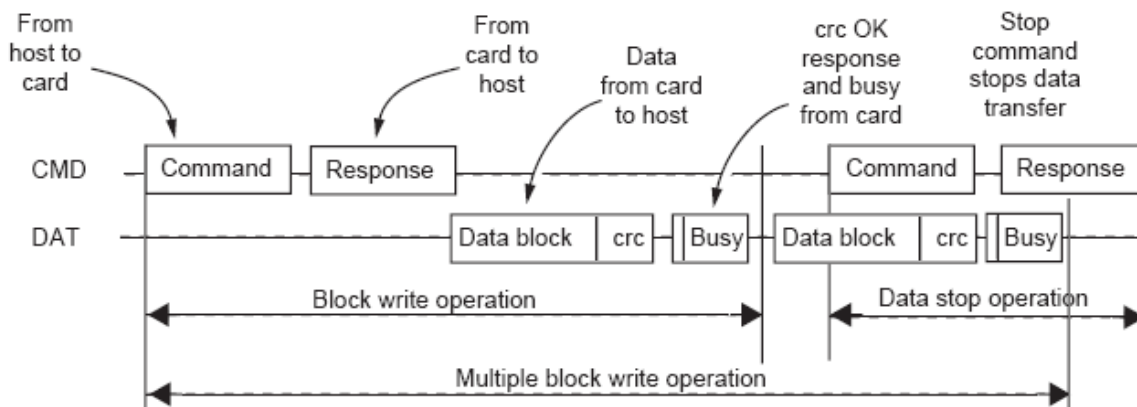


Figure 14 : Multiple Block Write Operation

Command tokens have the coding scheme shown in Figure 15.

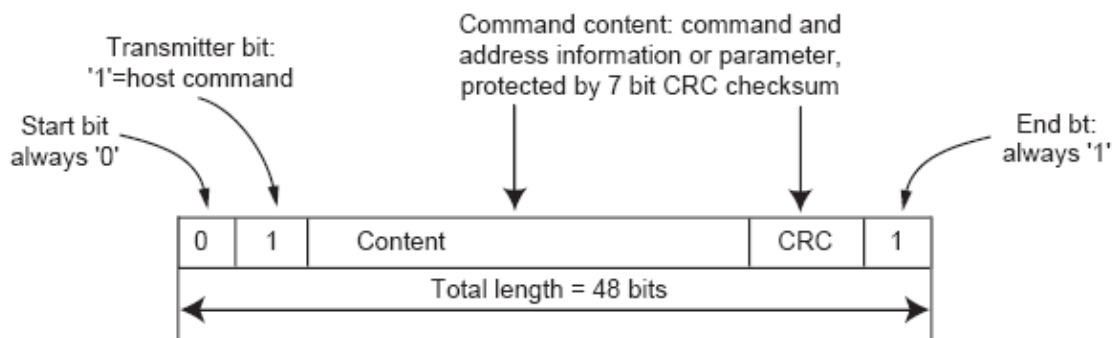


Figure 15 : Command Token Format

Each command token is preceded by a start bit ('0') and succeeded by an end bit ('1'). The total length is 48 bits. Each token is protected by CRC bits so that transmission errors can be detected and the operation may be repeated. Response tokens have four coding schemes depending on their content. The token length is either 48 or 136 bits. The CRC protection algorithm for block data is a 16-bit CCITT polynomial.

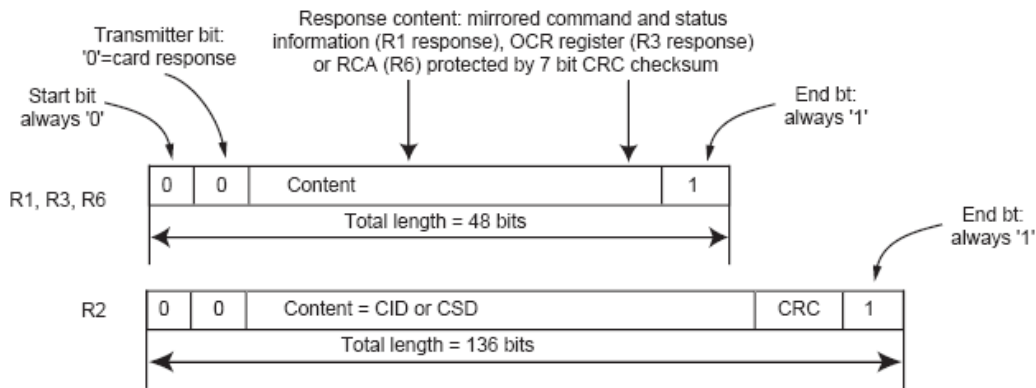


Figure 16 : Response Token Format

In the CMD line, the MSB bit is transmitted first, whereas the LSB bit is transmitted last.

When the wide bus option is used, the data is transferred 4 bits at a time (see Figure 17). Start and end bits, as well as the CRC bits, are transmitted for every one of the DAT lines. CRC bits are calculated and checked for every DAT line individually. The CRC status response and Busy indication will be sent by the card to the host on DAT0 only (DAT1-DAT3 during that period are "don't care").

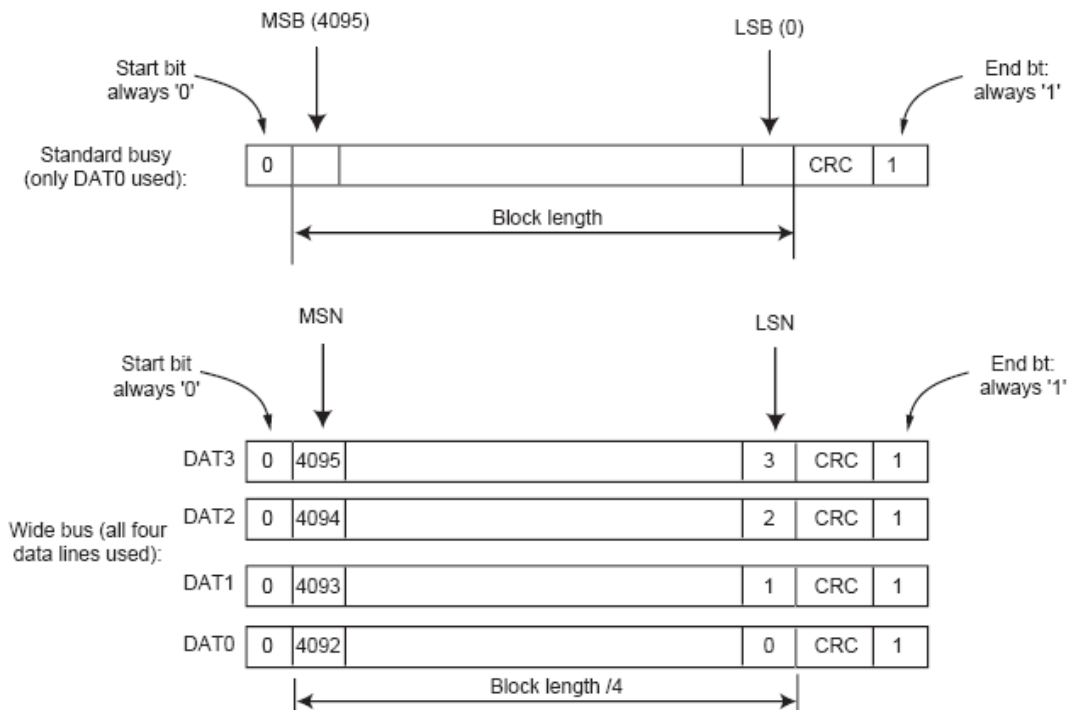


Figure 17 : Data Packet Format

6. SPI Protocol Definition

6.1. SPI Bus Protocol

While the Industrial Grade SD Card channel is based on command and data bit-streams, which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of eight bit bytes and is byte aligned (multiples of eight clocks) to the CS signal.

Similar to the SD Bus protocol, the SPI messages are built from command, response and data-block tokens. All communication between host and cards is controlled by the host (master). The host starts every bus transaction by asserting the CS signal low.

The response behavior in SPI Bus mode differs from the SD Bus mode in the following three ways:

- The selected card always responds to the command.
- An eight or 16-bit response structure is used.
- When the card encounters a data retrieval problem, it will respond with an error response (which replaces the expected data block) rather than time-out as in the SD Bus mode.

In addition to the command response, every data block sent to the card during write operations will be responded with a special data response token. A data block may be as big as one card write block (WRITE_BL_LEN) and as small as a single byte.¹

Note : 1) The default block length is as specified in the CSD (512 bytes). A set block length of less than 512 bytes will cause a write error. The only valid write set block length is 512 bytes. CMD16 is not mandatory if the default is accepted.

6.1.1. Data Read

SPI mode supports single block and multiple block read operations (SD Card CMD17 or CMD18). Upon reception of a valid read command the card will respond with a response token followed by a data token in the length defined in a previous SET_BLOCK_LENGTH (CMD16) command (see Figure 18).

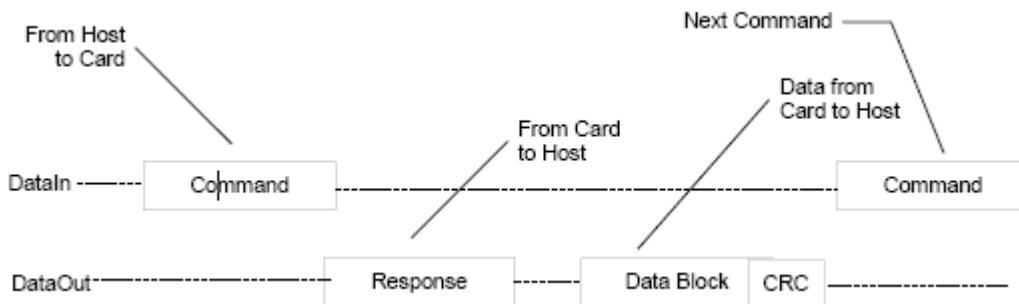


Figure 18 : Single Block Read Operation

A valid data block is suffixed with a 16-bit CRC generated by the standard CCITT polynomial:

$$x^{16}+x^{12}+x^5+1.$$

The maximum block length is 512 bytes as defined by READ_BL_LEN (CSD parameter). Block lengths can be any number between 1 and READ_BL_LEN.

The start address can be any byte address in the valid address range of the card. Every block, however, must be contained in a single physical card sector.

In case of data retrieval error, the card will not transmit any data. Instead, a special data error token will be sent to the host. Figure 19 shows a data read operation, which terminated with an error token rather than a data block.

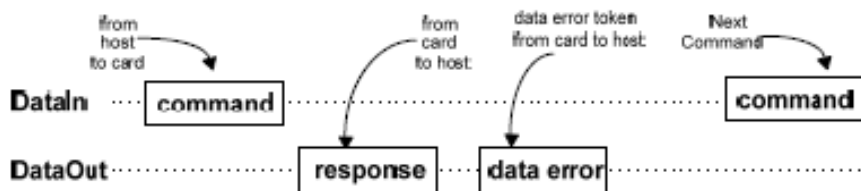


Figure 19 : Read Operation—Data Error

In the case of a Multiple Block Read operation, every transferred block has a 16-bit CRC suffix. The Stop Transmission command (CMD12) will actually stop the data transfer operation (the same as in SD Bus mode).

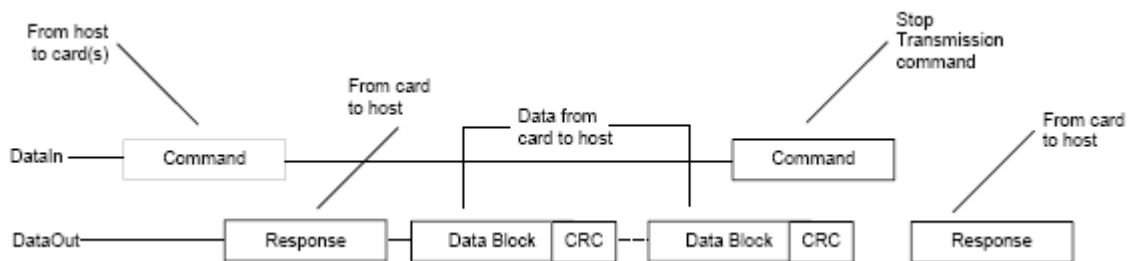


Figure 20 : Multiple Block Read Operation

6.1.2. Data Write

In SPI mode, the Industrial Grade SD Card supports single block or multiple block write operations. Upon reception of a valid write command (SD Card CMD24 or CMD25), the card will respond with a response token and will wait for a data block to be sent from the host. CRC suffix and start address restrictions are identical to the read operation (see Figure 21). The only valid block length, however, is 512 bytes. Setting a smaller block length will cause a write error on the next write command.

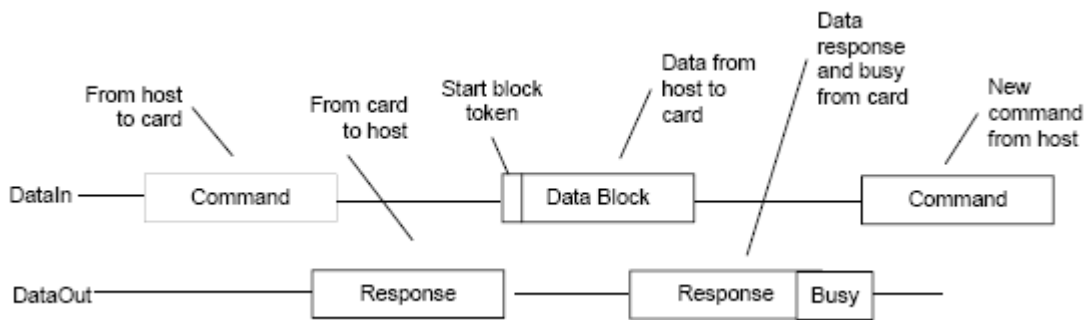


Figure 21 : Single Block Write Operation

Every data block has a prefix or 'start block' token (one byte). After a data block is received the card will respond with a data-response token, and if the data block is received with no errors, it will be programmed. As long as the card is busy programming, a continuous stream of busy tokens will be sent to the host (effectively holding the dataOut line low).

Once the programming operation is completed, the host must check the results of the programming using the SEND_STATUS command (CMD13). Some errors (e.g., address out of range, write protect violation, etc.) are detected during programming only. The only validation check performed on the data block and communicated to the host via the data-response token is CRC and general Write Error indication.

In Multiple Block write operation the stop transmission will be done by sending 'Stop Tran' token instead of 'Start Block' token at the beginning of the next block. In case of Write Error indication (on the data response) the host shall use SEND_NUM_WR_BLOCKS (ACMD22) in order to get the number of well written write blocks

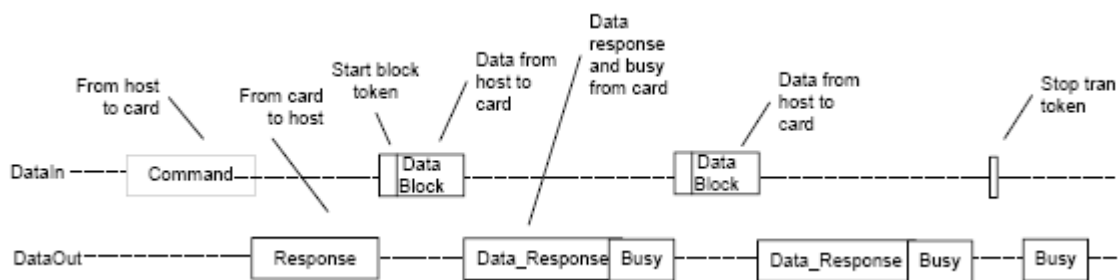


Figure 22 : Multiple Block Write Operation

Resetting the CS signal while the card is busy does not terminate the programming process. The card releases the dataOut line (tristate) and continues to program. If the card is reselected before the programming is done, the dataOut line will be forced back to low and all commands will be rejected.


Resetting a card (using CMD0) will terminate any pending or active programming operation. This may destroy the data formats on the card. It is the host's responsibility to prevent it.

Appendix A. Ordering Information

Industrial Secure Digital (SD) Memory Card

Operating temperature supports Industrial grade -40°C ~ 85°C

Part number list :

Product Picture	Capacity	-40° C~ 85° C
	128MB	WPSDC128M-IAISI
	256MB	WPSDC256M-IAISI
	512MB	WPSDC512M-IAISI
	1GB	WPSDC001G-IAISI
	2GB	WPSDC002G-IAISI

Part number decoder :

X1 X2 X3 X4 X5 X6 X7 X8 X9 X11 X12 X13 X14 X15

X1 : Grade

W : Industrial grade – operating temp. -40° C ~ 85 ° C

X11 : Controller

I : InCOMM

X2 : The material of case

P : Plastic casing

X12 : Controller version

A,B,C.....

X3 X4 X5 : Product category

SDC : Secure Digital (SD) memory card

X13 : Controller grade

I : Industrial grade

X6 X7 X8 X9 : Capacity

128M: 128MB

256M: 256MB

512M: 512MB

001G: 1GB

002G: 2GB

X14 : Flash IC

S : Samsung SLC-NAND Flash IC

X15 : Flash IC grade / Type

I : Industrial grade

Appendix B. Limited Warranty

APRO warrants your Industrial SD Memory Cards against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO .

Product shall be returned to with shipping prepaid. If the product fails to conform based on customers' purchasing orders, will reimburse customers for the transportation charges incurred.